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SESSION 2

RF Frequency Synthesis Techniques

An Integrated 0.56THz Frequency Synthesizer with 21GHz Locking Range and -74dBc/Hz Phase Noise at 1MHz Offset in 65nm CMOS

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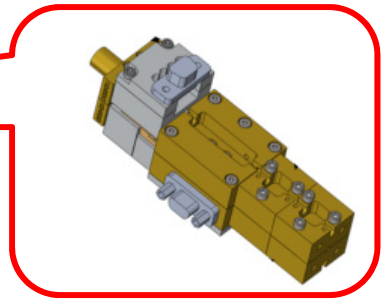
Outline

- Motivation and Challenges
- Design Concepts
  - THz VCOs
  - Frequency dividers
  - Wideband tuning front-end
  - Back-end
- Implementation and measurement
- Conclusion

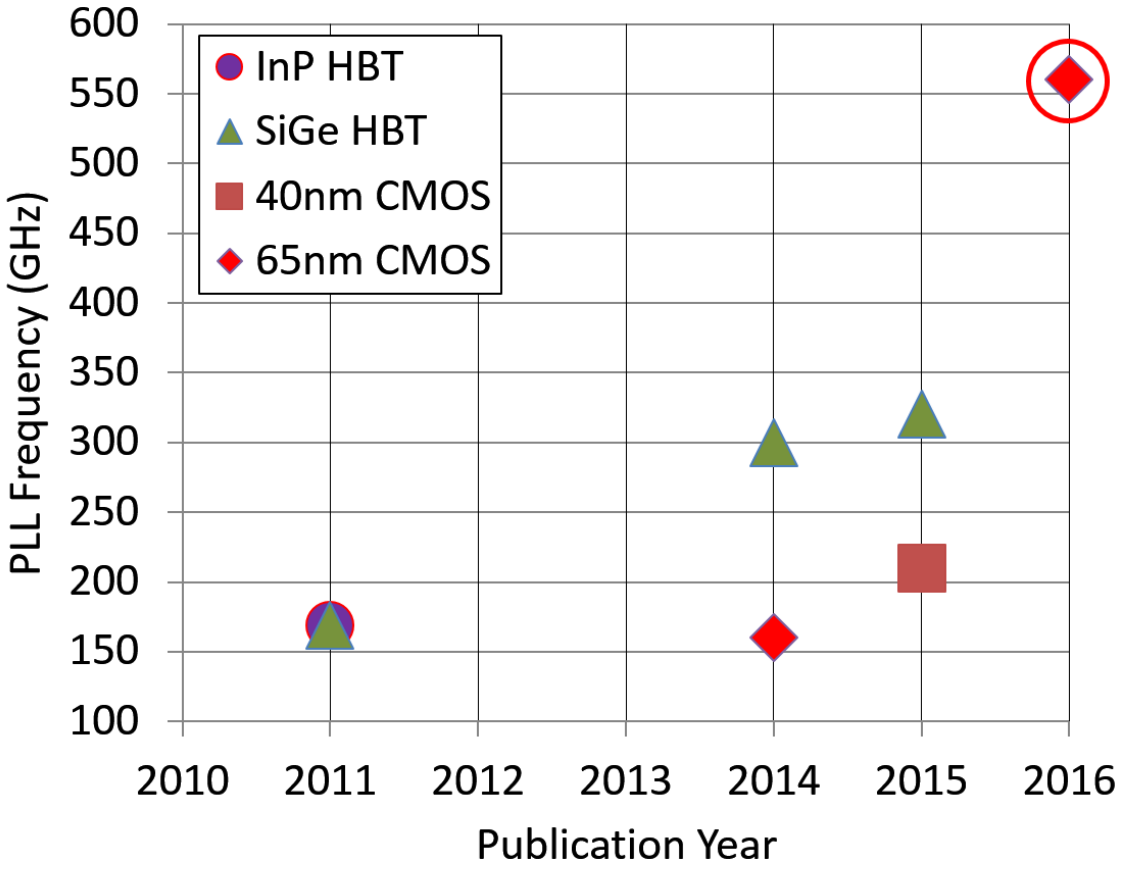
Motivation

- Absorption spectra from 0.5 to 0.6THz
- Detection of water, and organics (CH4 and HCN)
- Existing JPL waveguide LO chain (33GHz PLL, x3, x2, and x3 frequency multipliers, 2.5kg, 3000cm^3, 11.5W)
- Proposed 0.56THz CMOS PLL chip for low weight, size and energy consumption



Prior PLL Arts in (Sub)-mm Wave Bands

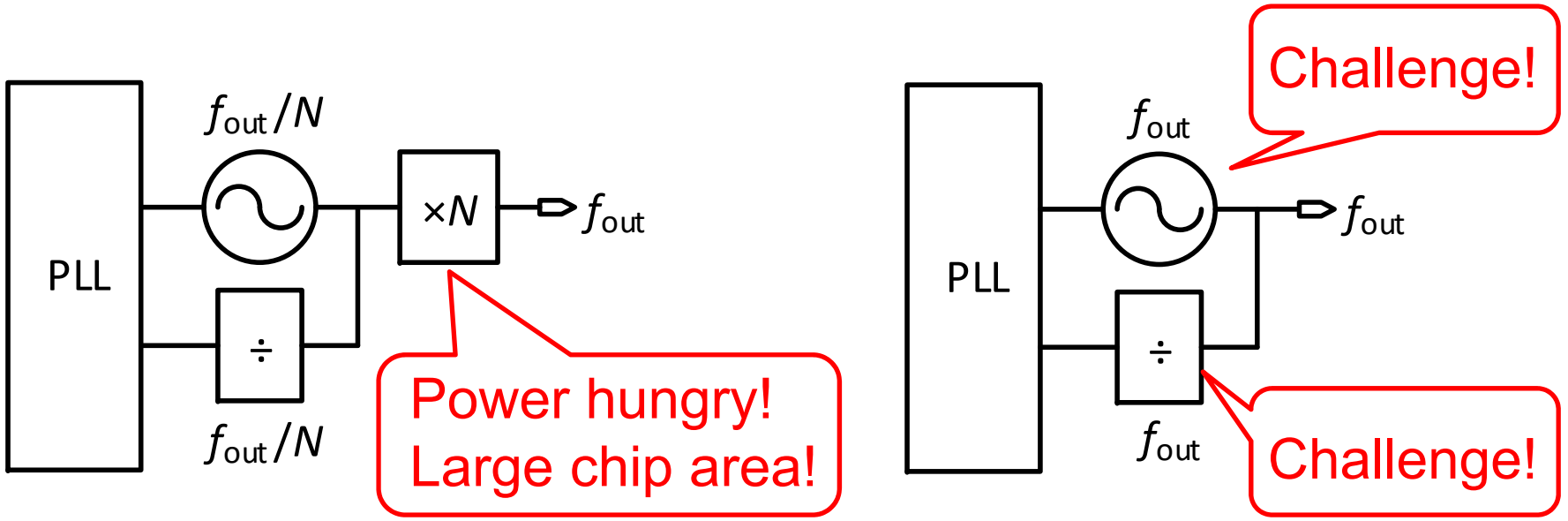
- HBT
  - ✓ InP: 300GHz PLL
  - ✓ SiGe: 300GHz PLL
- CMOS
  - ✓ 40nm: 210GHz PLL
  - ✓ 65nm: 160GHz PLL



This work:
560GHz PLL
in 65nm CMOS

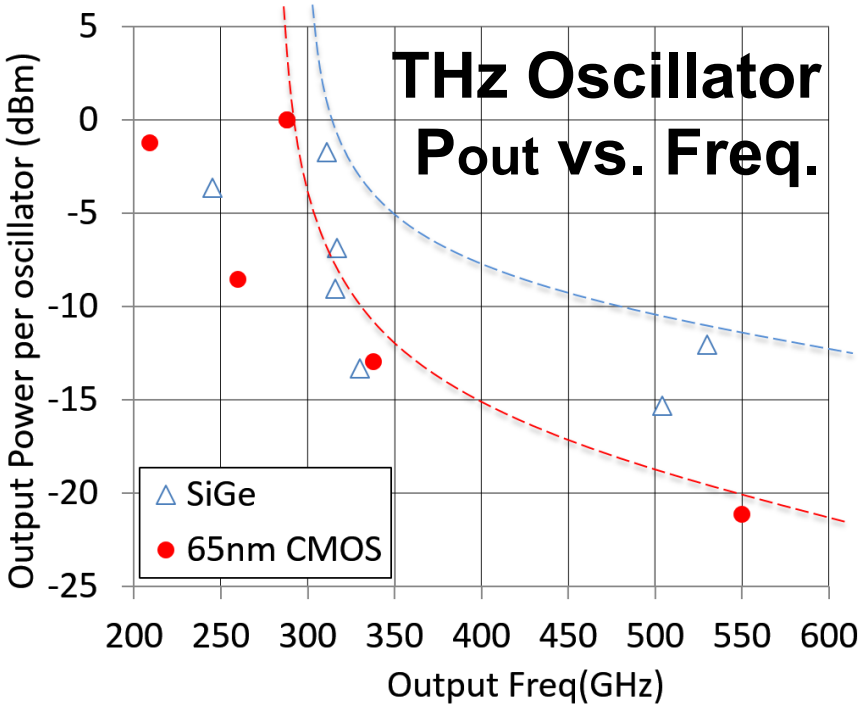
Phase Locking at Terahertz (>300GHz)

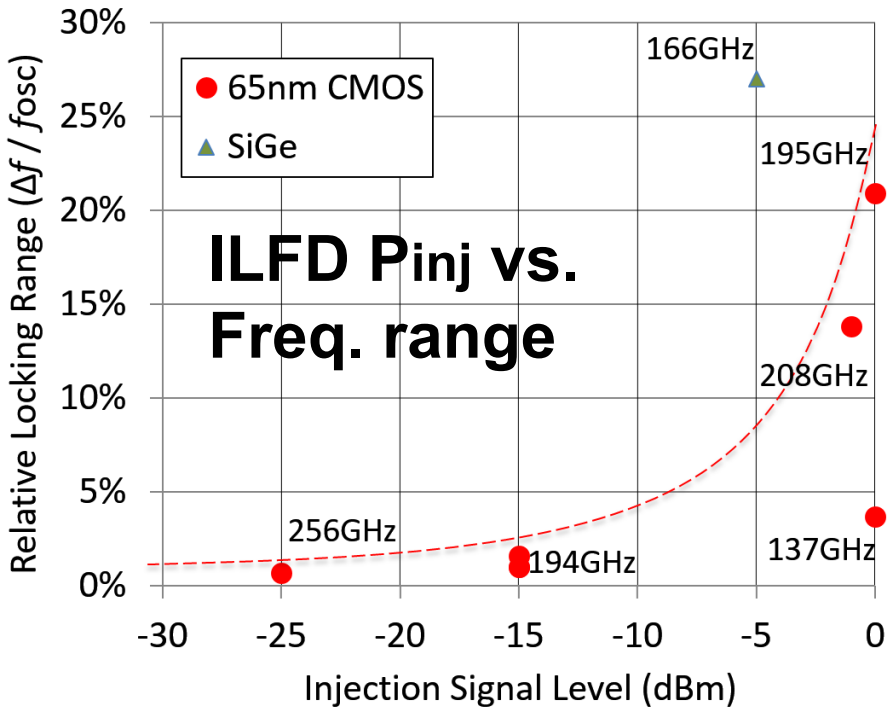
- Lower frequency VCO + Frequency multipliers
  - High power consumption
  - Large chip area
- Higher frequency VCO + Frequency divider
  - Challenging oscillator design
  - Challenging divider design



THz Oscillators and Dividers Overview

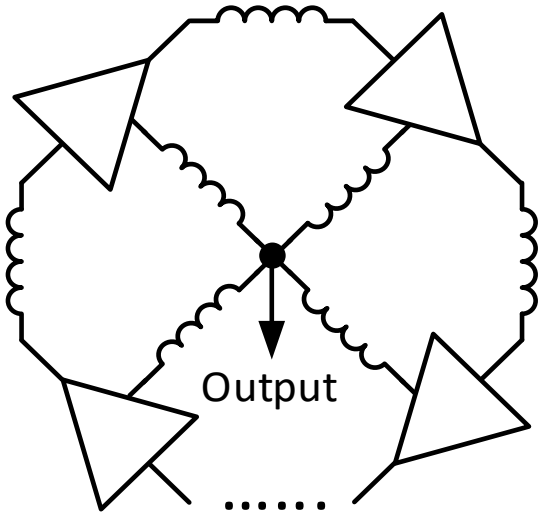
- CMOS Oscillator > 500GHz
  - P_{out}< -20dBm per oscillator
- CMOS Injection Locking Frequency Divider (ILFD)
  - <256GHz with diminishing locking range





Ring-Type Oscillators

- Ring-Type Oscillator with Multi-Push Output
  - Output power enhanced by boosting harmonics
  - More compact circuit size



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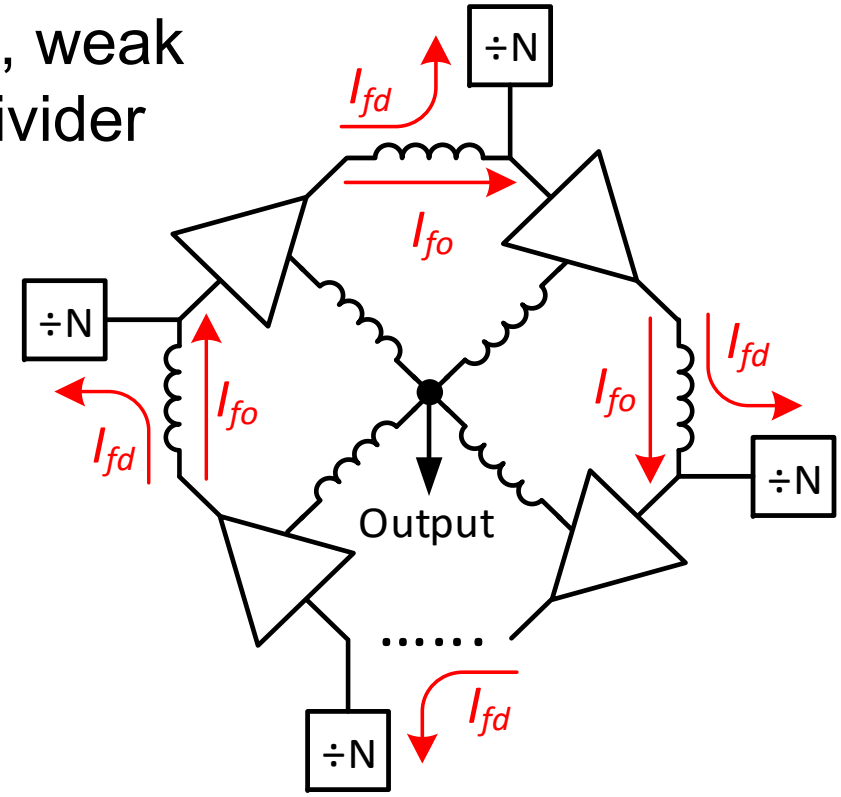
  - Option 1: direct coupling, weak oscillator swing due to divider loading



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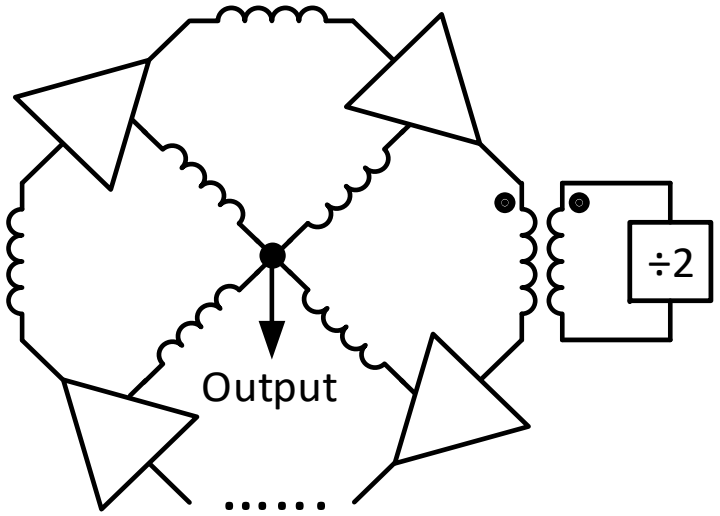
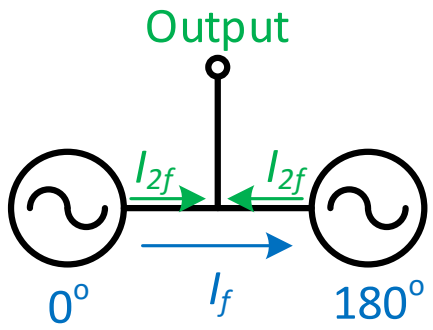
  - Option 2: magnetic coupling, hard to lock divider due to high coupling loss at (sub) mm-wave frequencies



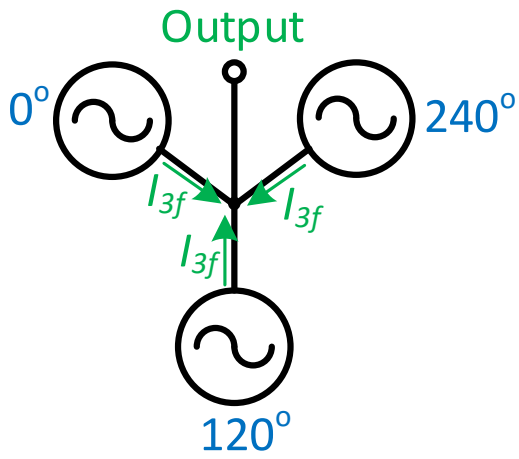
Star-Type Oscillators

Identical oscillators coupled in multifold symmetries



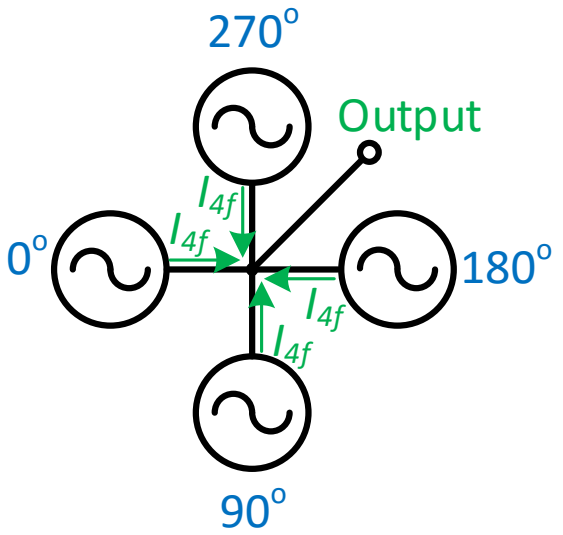
$0^o \times 2 = 0^o$
$180^o \times 2 = 0^o$

280GHz x 2 = 0.56THz
Divider Oscillator



$0^o \times 3 = 0^o$
$120^o \times 3 = 0^o$
$240^o \times 3 = 0^o$

187GHz x 3 = 0.56THz
Divider Oscillator

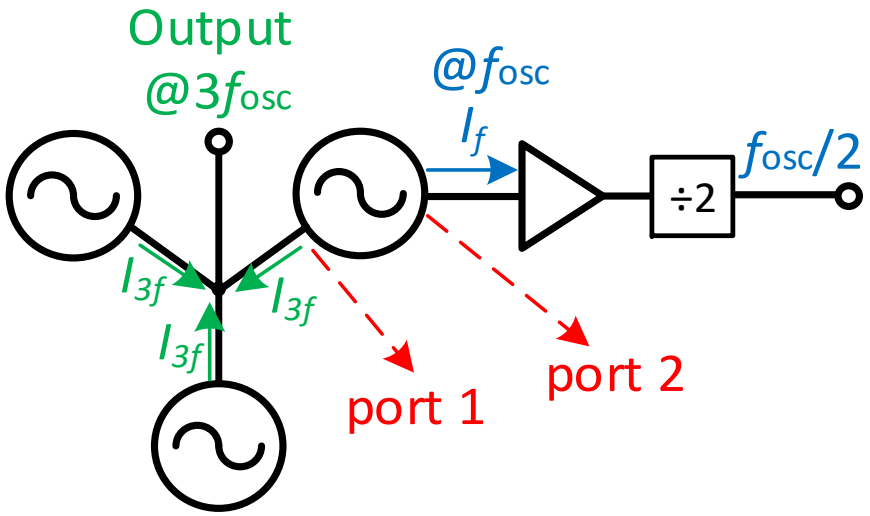


$0^o \times 4 = 0^o$
$90^o \times 4 = 0^o$
$180^o \times 4 = 0^o$
$270^o \times 4 = 0^o$

140GHz x 4 = 0.56THz
Divider Oscillator

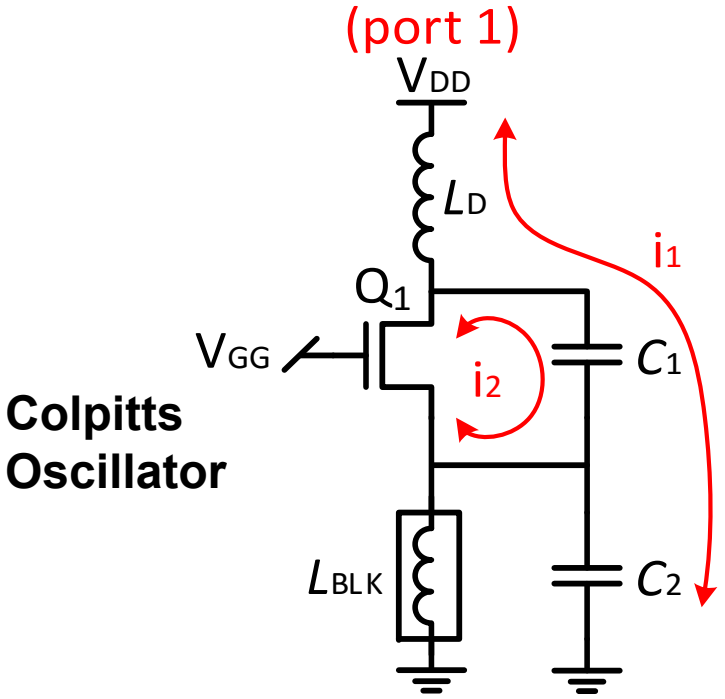
Star-Type Oscillator with 3-fold Symmetry

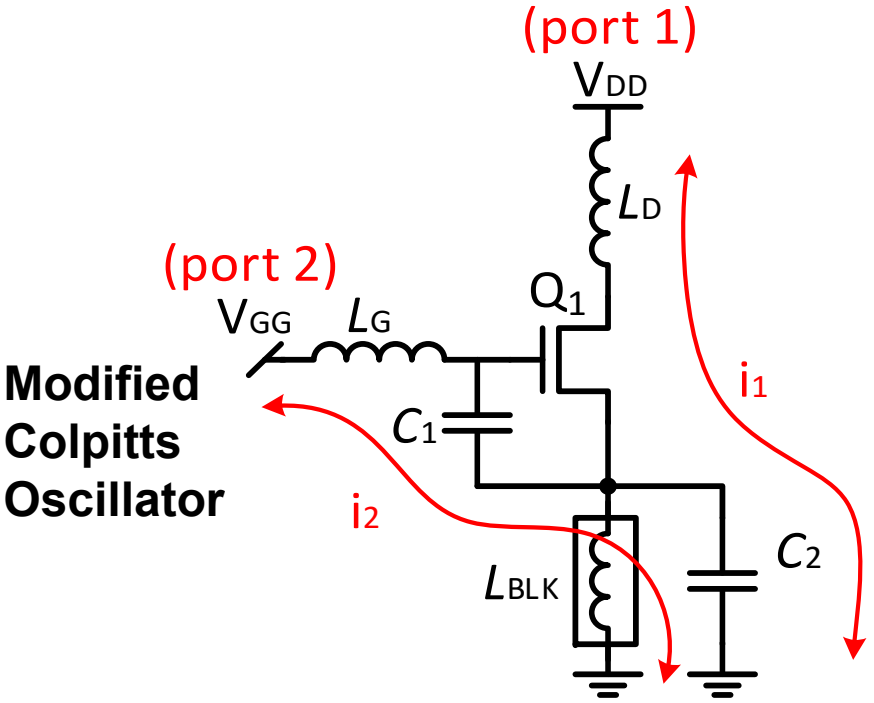
- Three-fold symmetrically coupled oscillators
  - Combining 3rd harmonic in-phase currents from 3 individual oscillators to output
  - Coupling to divider chain via one oscillator at the fundamental frequency
- Advantages
  - Combining 3rd harmonic signals at port 1 with enhanced P_{out}
  - Securing wider locking range by injecting higher signal level at fundamental frequency through the 2nd port



THz Oscillator Circuitry

- Traditional Colpitts Oscillator
  - Inductor at drain
  - One port (V_{DD}) carrying AC current
- Modified Colpitts Oscillator
  - Inductors at drain and gate
  - Two ports (V_{DD} and V_{GG}) carrying AC current

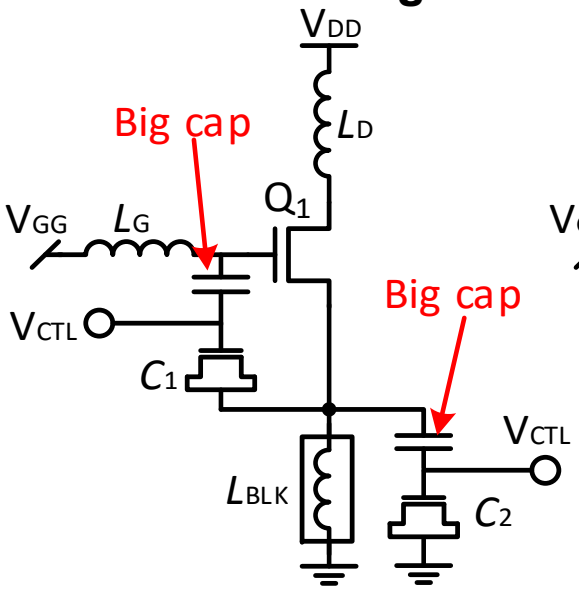




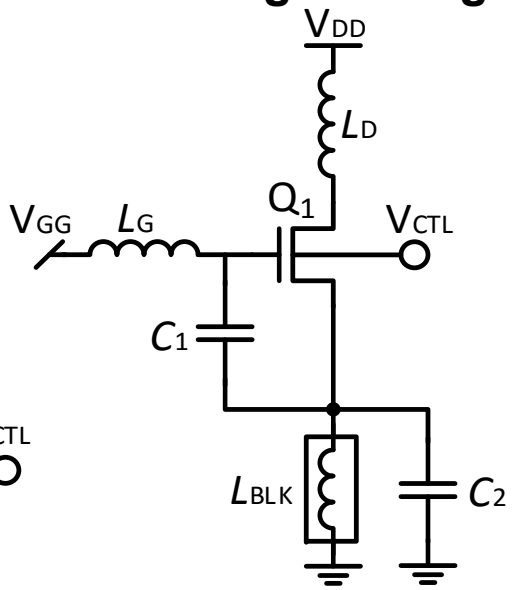
Terahertz VCO Frequency Tuning

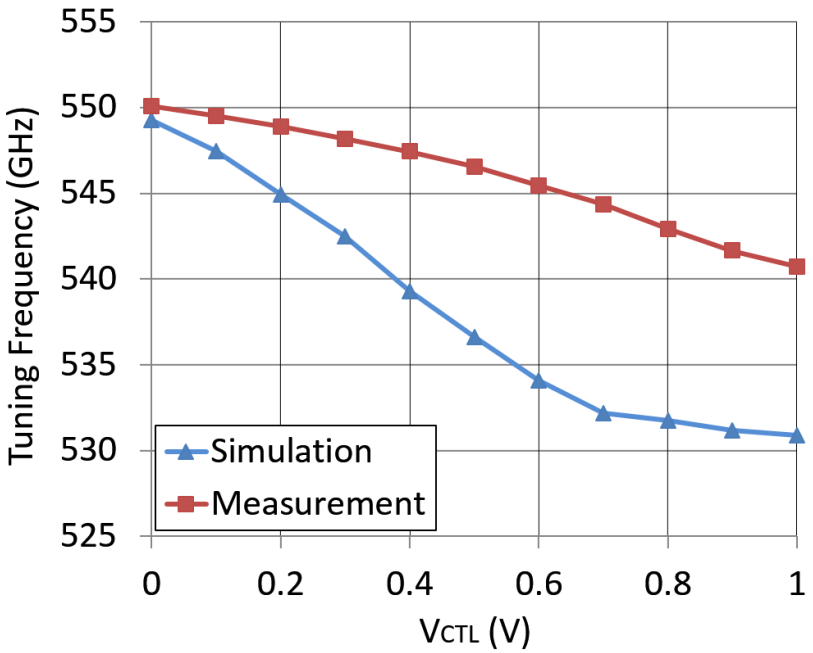
- Frequency Tuning
  - Varactor is not preferred
    - DC block cap required for voltage tuning
    - Low Q-factor at frequency of interest
  - Bulk voltage tuning
    - Simple circuit at minimum cost of Q-factor

Varactor Tuning



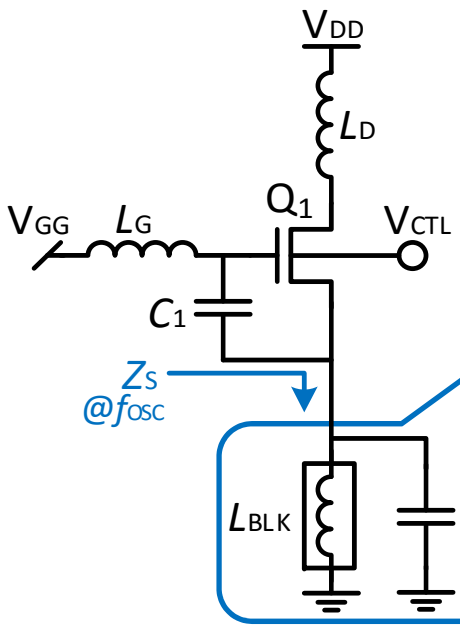
Bulk Voltage Tuning

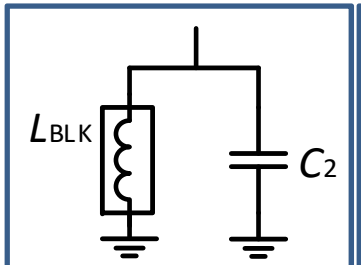




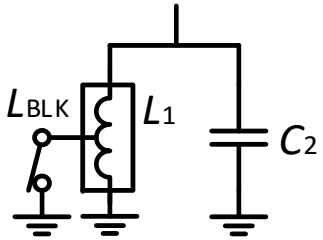
Boosting Terahertz VCO Tuning Range

- Varactor is not helpful
  - Low Q-factor
  - Limited tuning range
- Inductor switch
  - Truncating AC blocking inductor

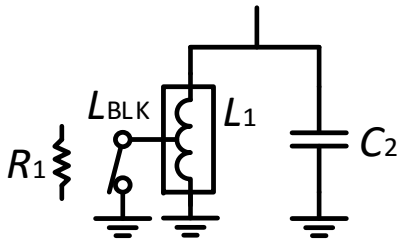




$$Z_S = \frac{1}{j\omega_{osc}C_2}$$



$$Z_S = \frac{1}{j\left(\omega_{osc}C_2 - \frac{1}{\omega_{osc}L_1}\right)}$$

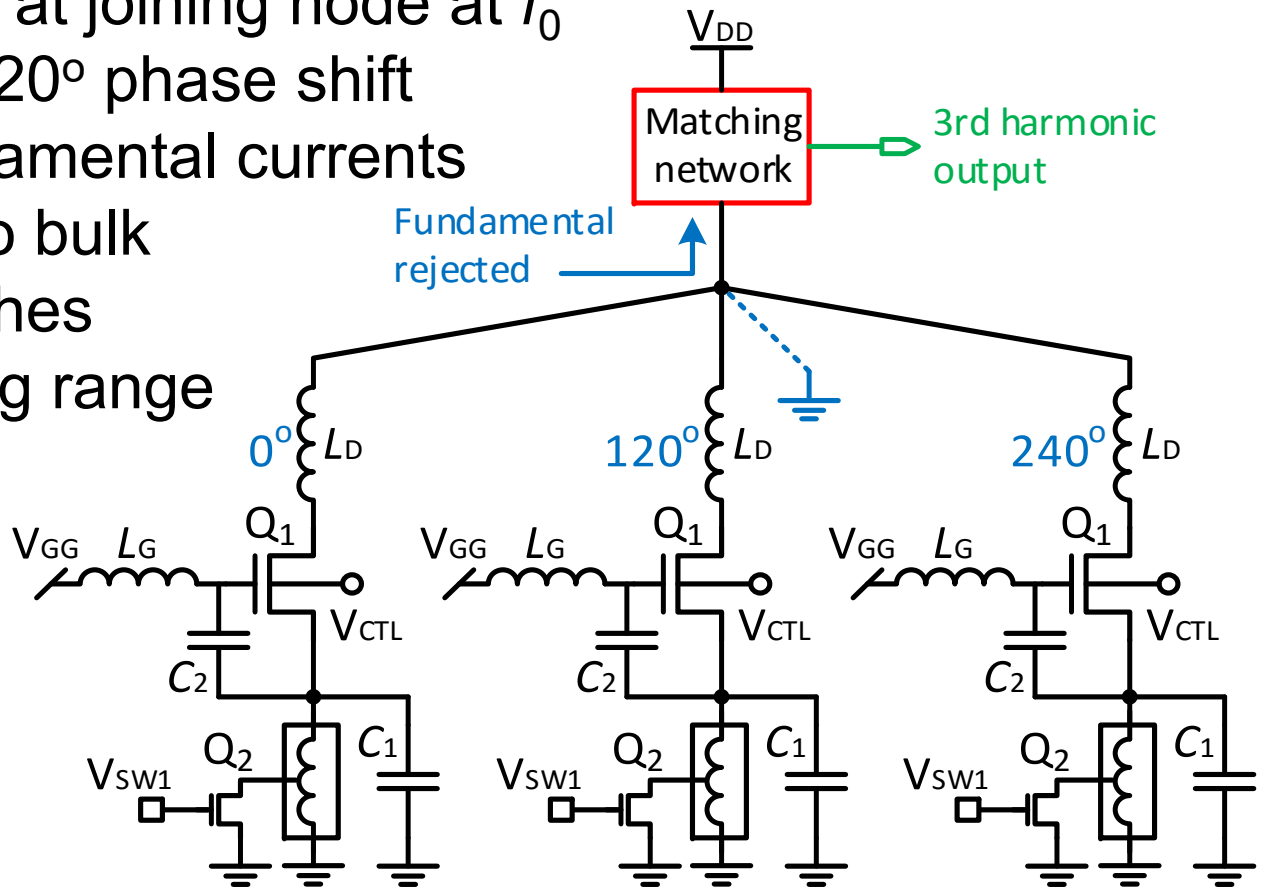


$$L_1 > \frac{1}{\omega_{osc}^2 C_2 - \omega_{osc} Q_0 R}$$

(Q_0 is required minimum Q-factor)

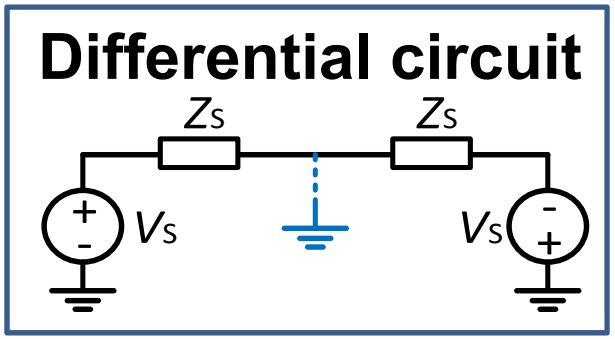
Proposed THz VCO Circuitry

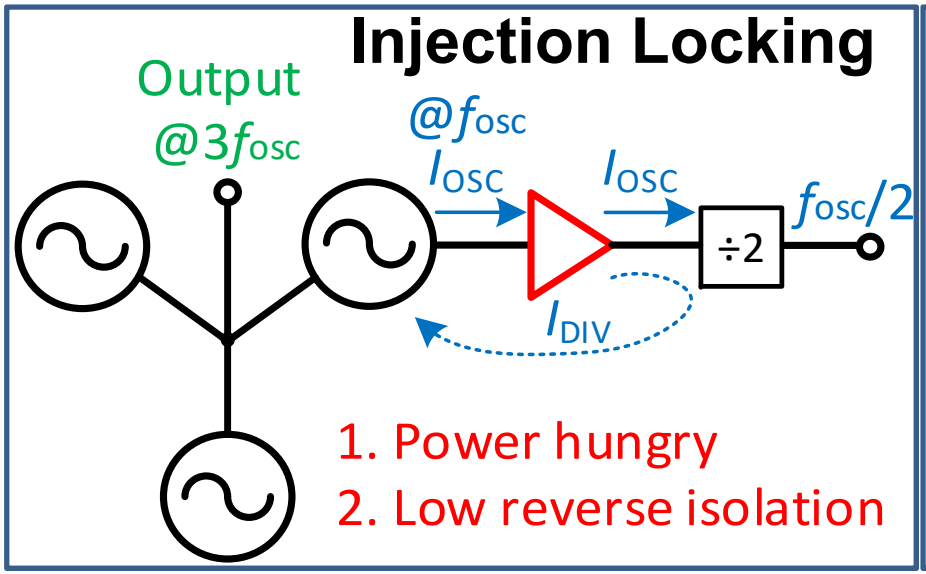
- Triple-push Colpitts VCO (TPCO)
  - 3 VCOs joined at V_{DD} port
  - Impedance matched at 3rd harmonic
  - Virtual ground at joining node at f_0
  - Progressive 120° phase shift among 3 fundamental currents
  - V_{CTL} applied to bulk
  - Inductor switches boosting tuning range

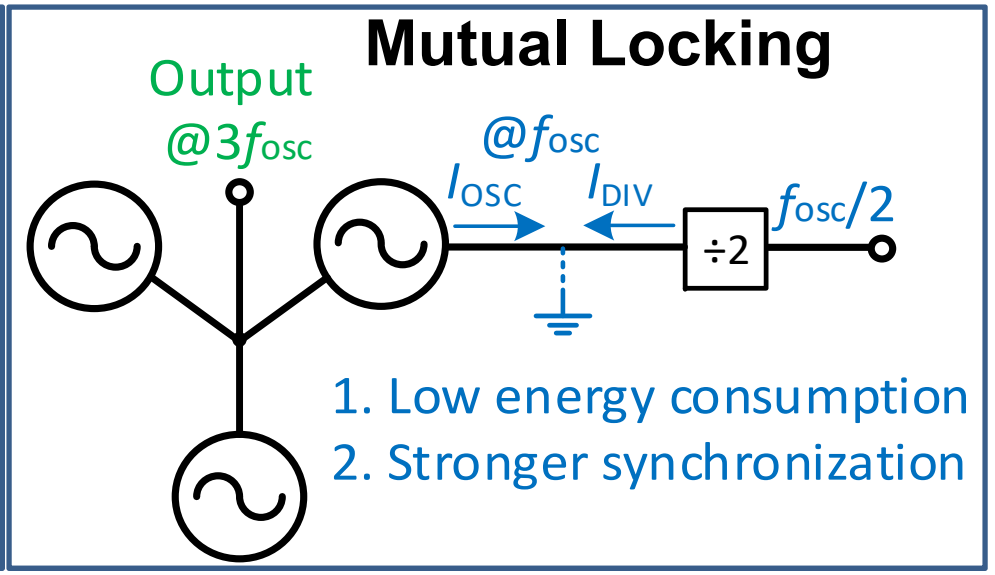


Proposed Mutual Locking

- Issues of injection locking
  - Low TPCO's swing requiring high gain buffer
  - Freq. pulling due to buffer's low reversion isolation at fund. freq. (~180GHz)
- Advantages of mutual locking
  - Avoid power hungry buffer
  - Stronger synchronization

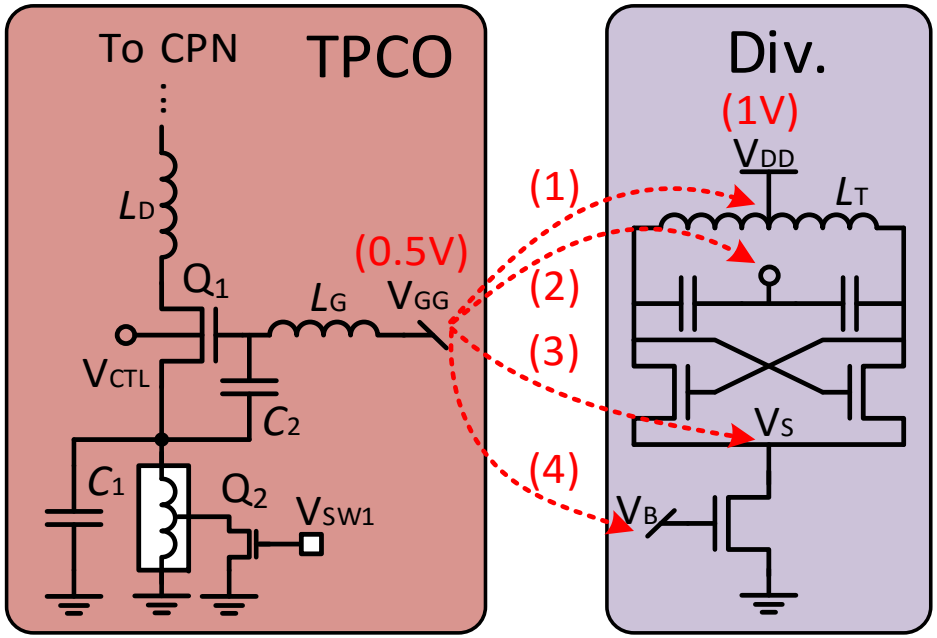






Mutual Locking Challenges

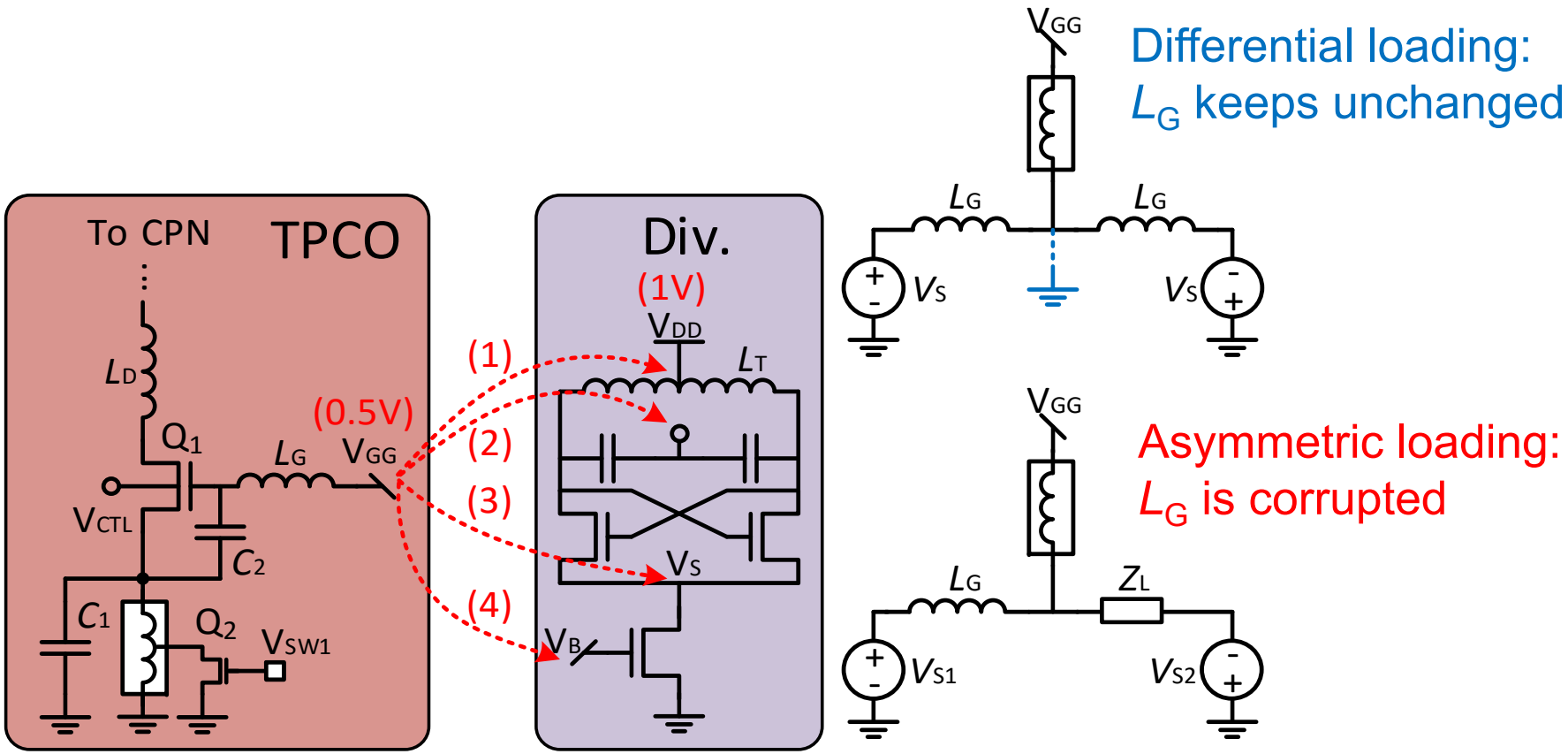
- Mutual locking between TPCO and cross-coupled divider
  - Unmatched DC voltages - (1)(3)



V_{GG}: 0.5V
V_{DD}: 1V
V_S: 0.6V

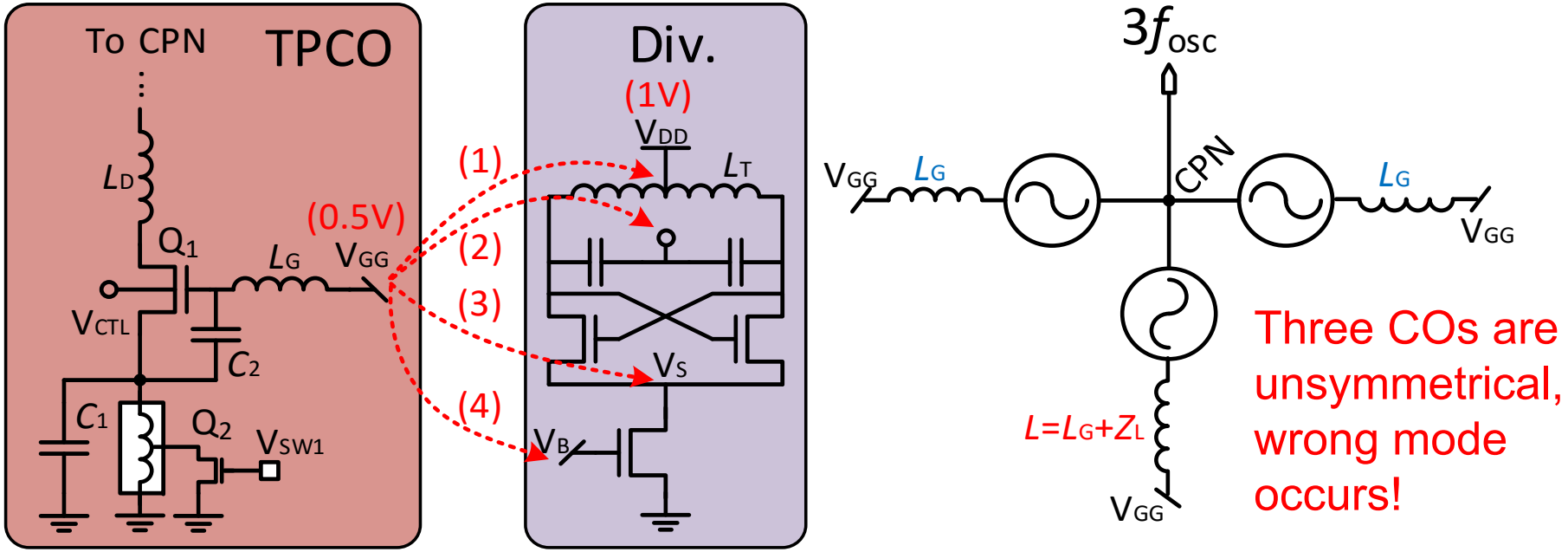
Mutual Locking Challenges

- Mutual locking between TPCO and cross-coupled divider
  - Unmatched DC voltages - (1)(3)
  - L_G Corruption - (2)(3)(4)



Mutual Locking Challenges

- Mutual locking between TPCO and cross-coupled divider
  - Unmatched DC voltages - (1)(3)
  - L_G Corruption - (2)(3)(4)
  - Unbalanced TPCO rendering wrong mode -(1)(2)(3)(4)



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- Mutual locking between TPCO and cross-coupled divider
  - Unmatched DC voltages - (1)(3)
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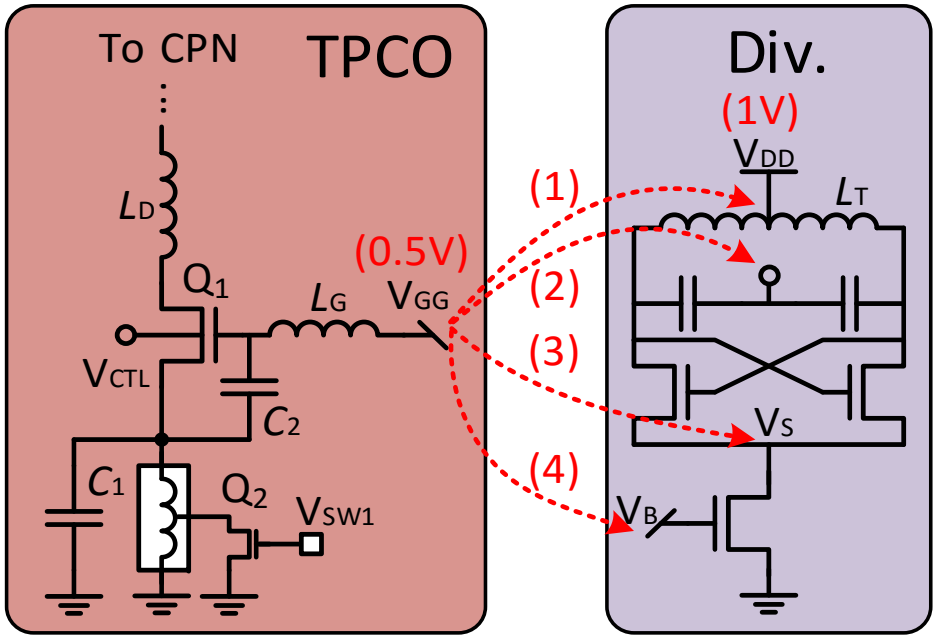
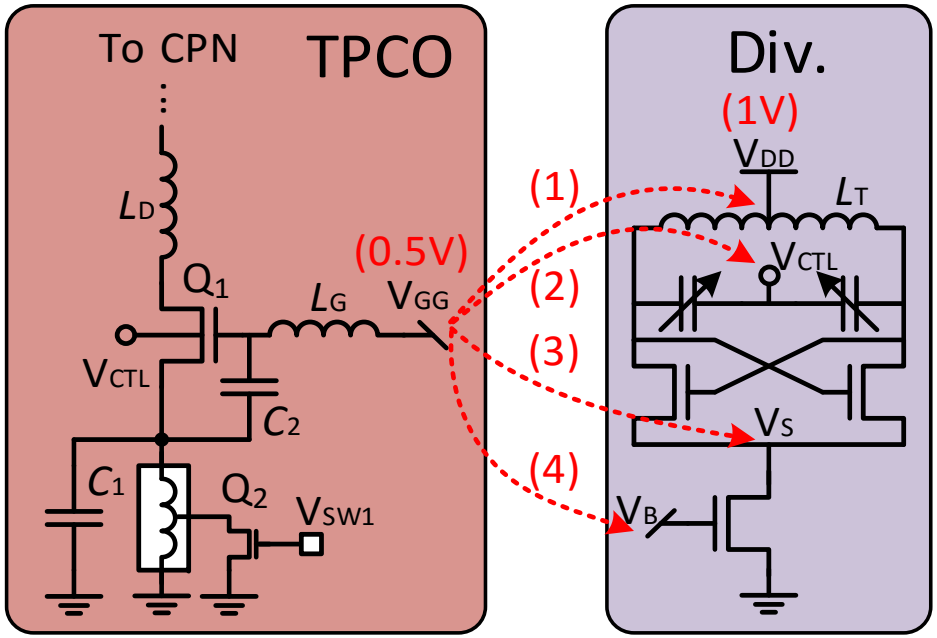
  - Narrow locking range - (1)(2)(3)(4)

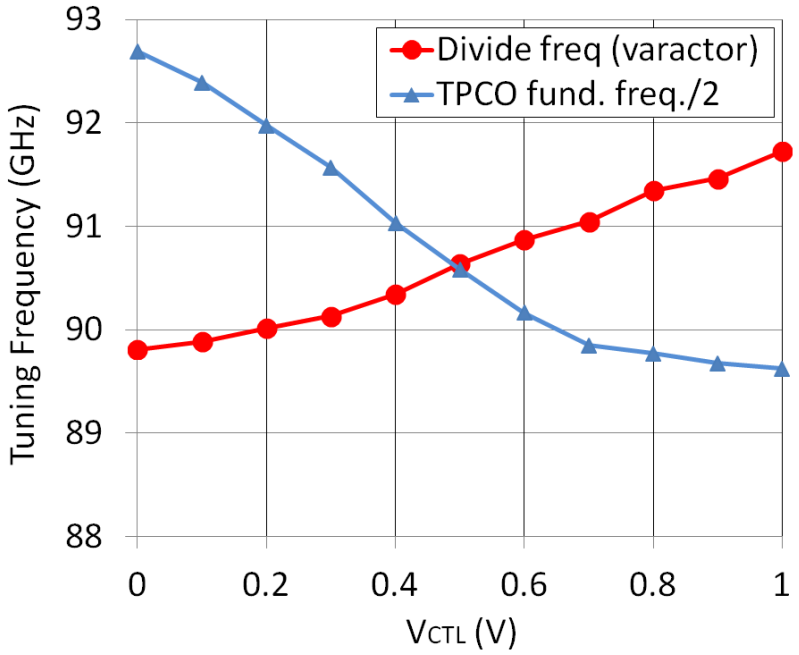


Time domain simulation shows less than 0.5GHz locking range with -5dBm signal injected into any of above four ports.

Mutual Locking Challenges

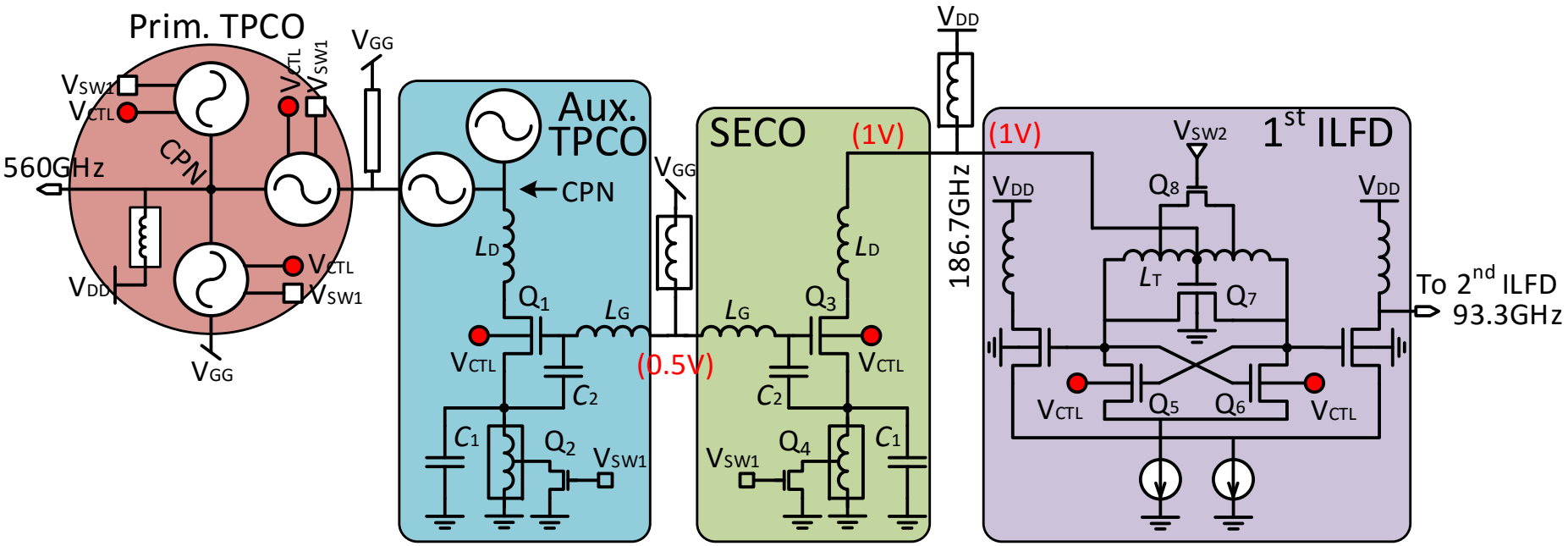
- Mutual locking between TPCO and cross-coupled divider
  - Unmatched DC voltages - (1)(3)
  - L_G Corruption - (2)(3)(4)
  - Unbalanced TPCO rendering wrong mode -(1)(2)(3)(4)
  - Narrow locking range - (1)(2)(3)(4)
  - Tuning curves mismatch - (1)(2)(3)(4)





Overall Locking Topology

- Inserting CO between TPCO and Divider for level shifting
- Inserting auxiliary TPCO to protect primary TPCO from entering wrong mode due to divider's asymmetric loading
- Locking 1st ILFD via two separate ports (L_T center tap and gate of switch Q_7 crossing L_T) to strengthen mutual locking



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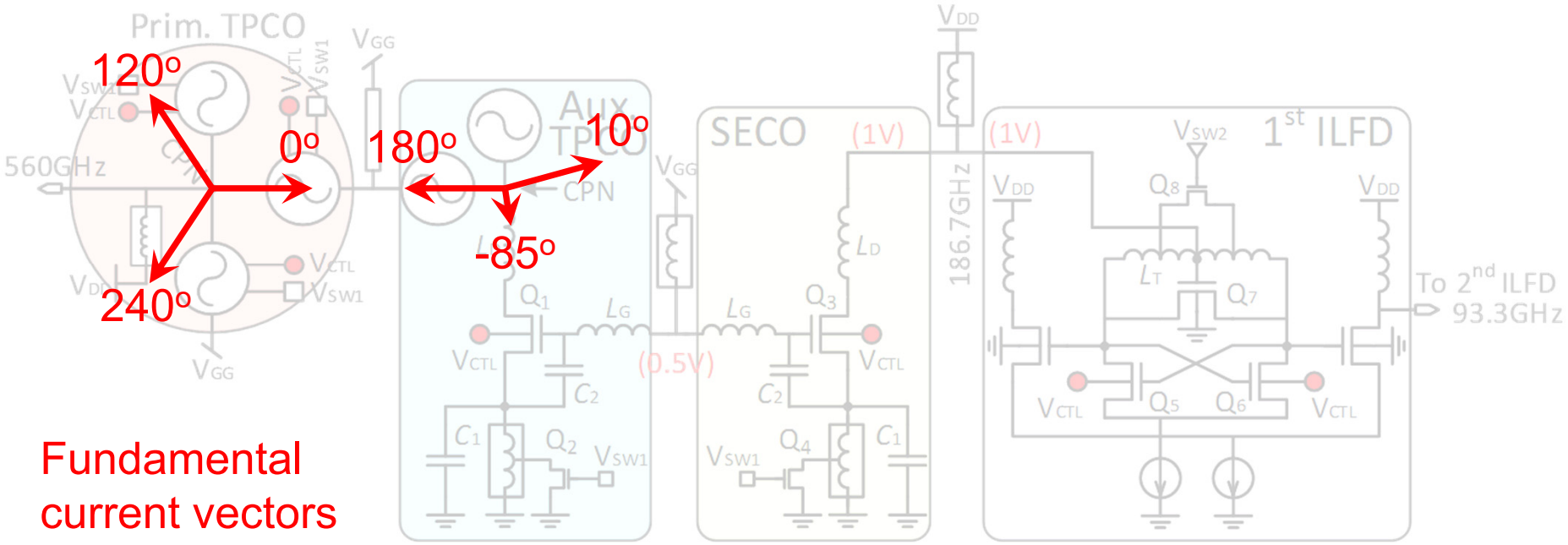
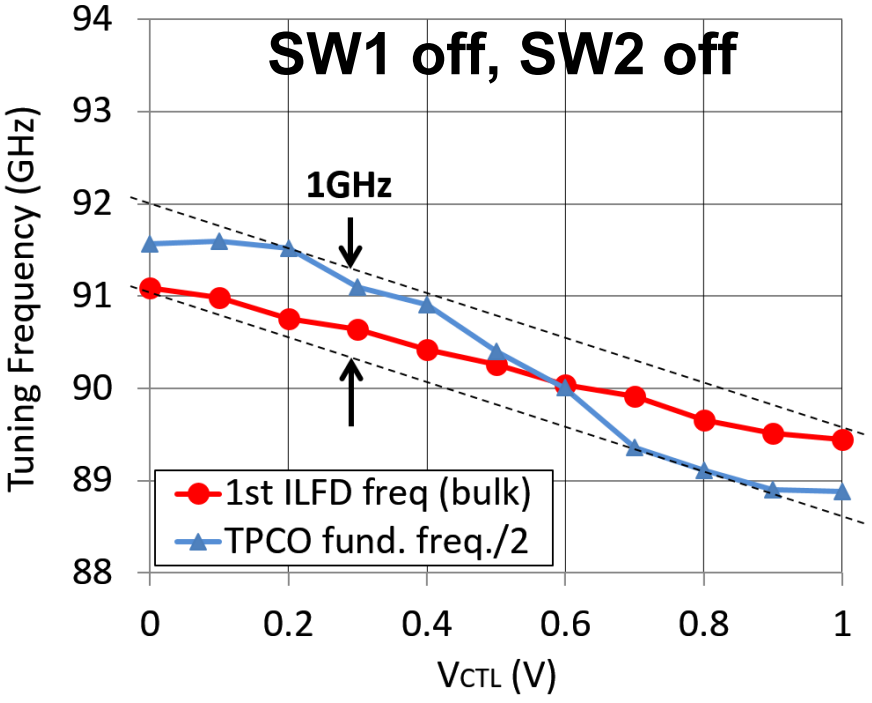
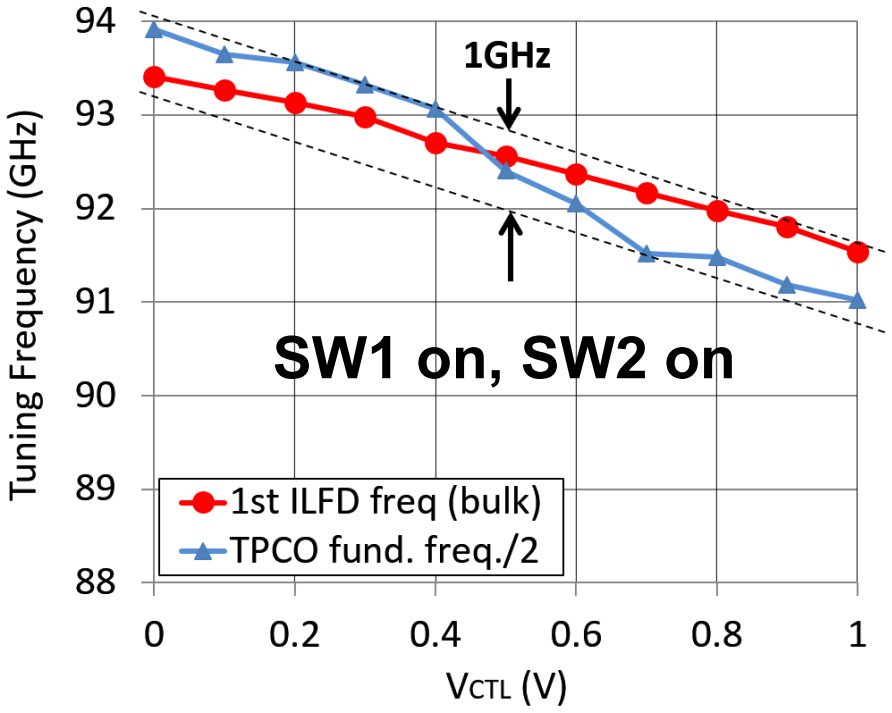


Overall Tuning Strategy

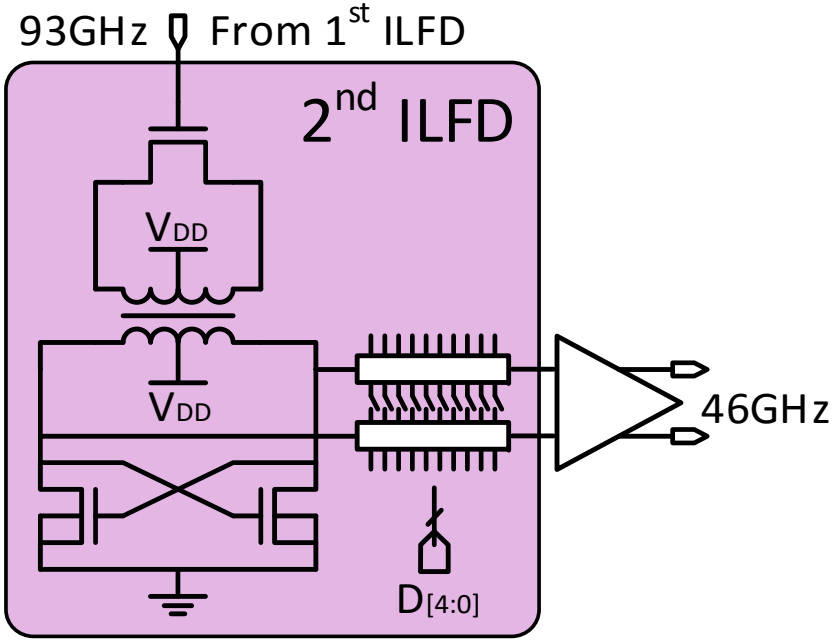
- Common V_{CTL} to all the blocks (primary TPCO, aux. TPCO, single-ended CO and 1st ILFD)
- TPCOs, CO and 1st ILFD locking range matched by adding a similar inductor switches Q2, Q4 and Q8
- Careful alignment of TPCO and 1st ILFD's tuning curves within 1GHz over tuning voltage range under all switches conditions

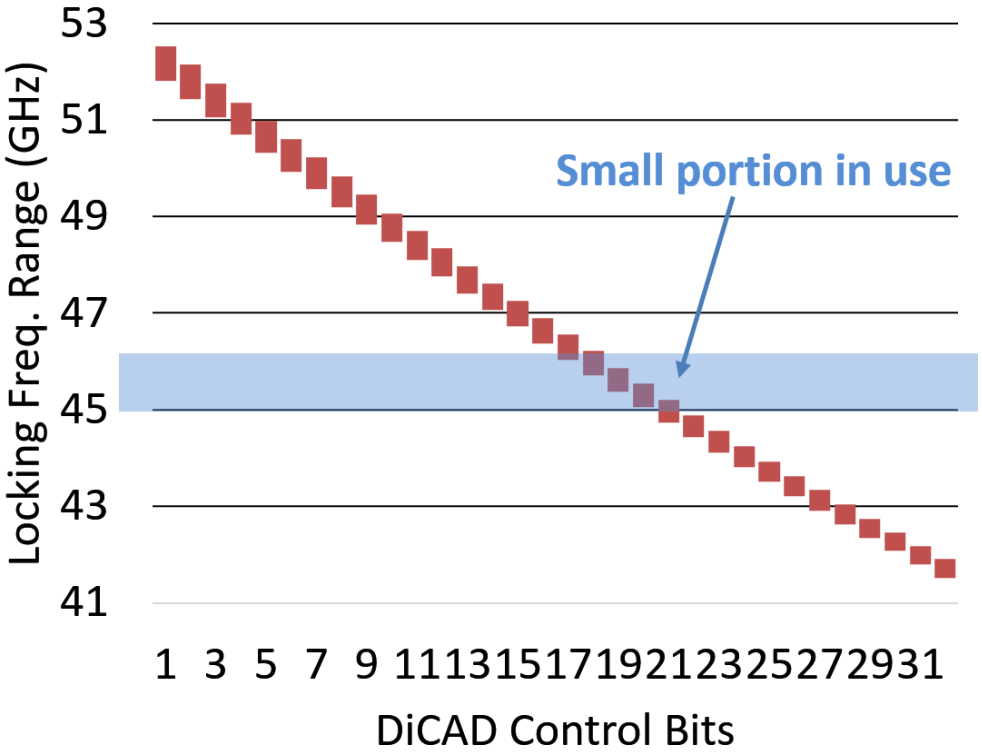




2nd Stage Divider

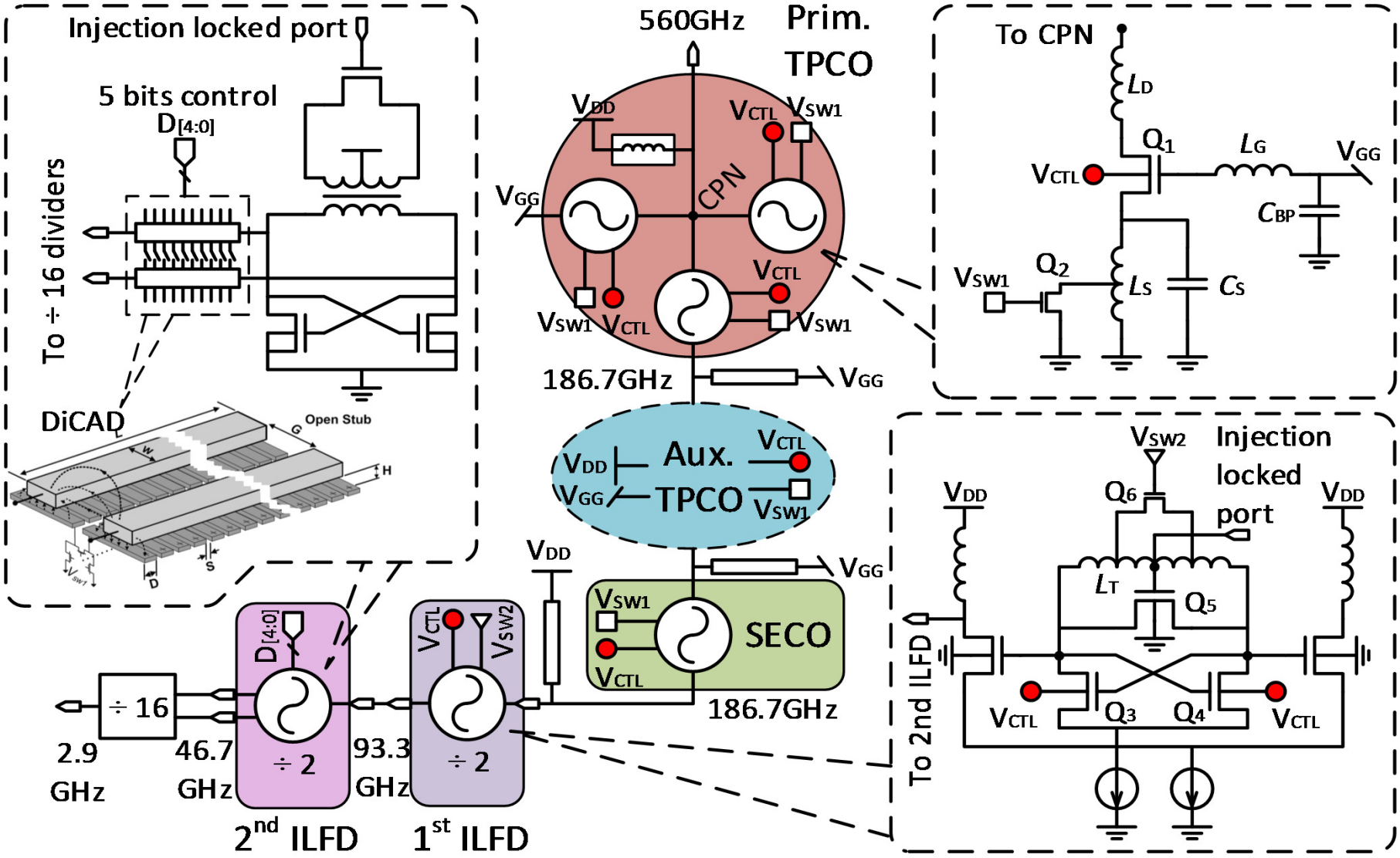
- DiCAD (Digital Controlled Artificial Dielectric) [La09] covering tuning range from 42 to 52.5GHz



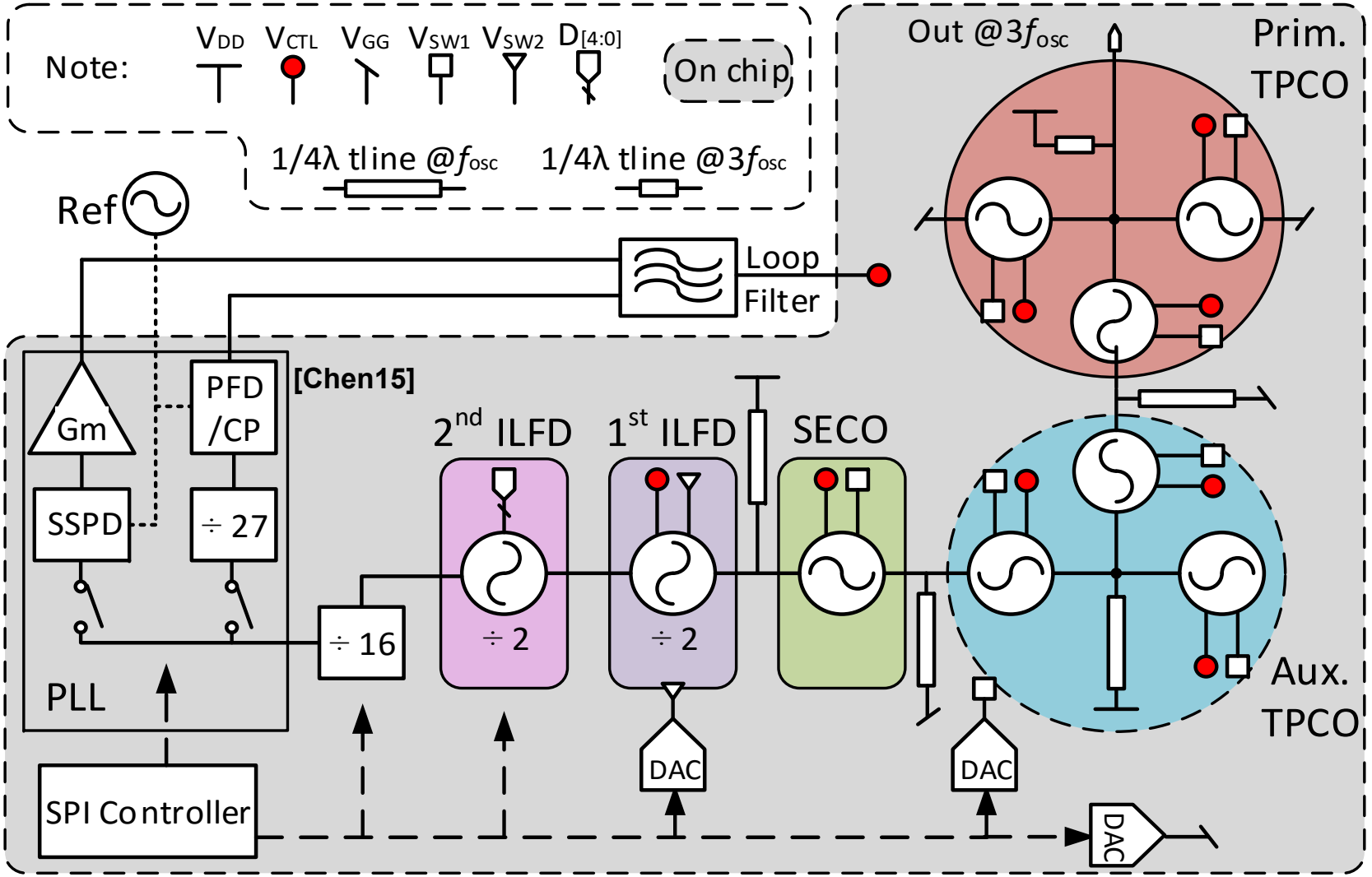


[La09] LaRocca, T. et al., "Embedded DiCAD linear phase shifter for 57-65GHz reconfigurable direct frequency modulation in 90nm CMOS", IEEE Symposium on Radio Frequency Integrated Circuits (RFIC 2009), pp.219-222, 7-9 June 2009

Terahertz PLL Front End



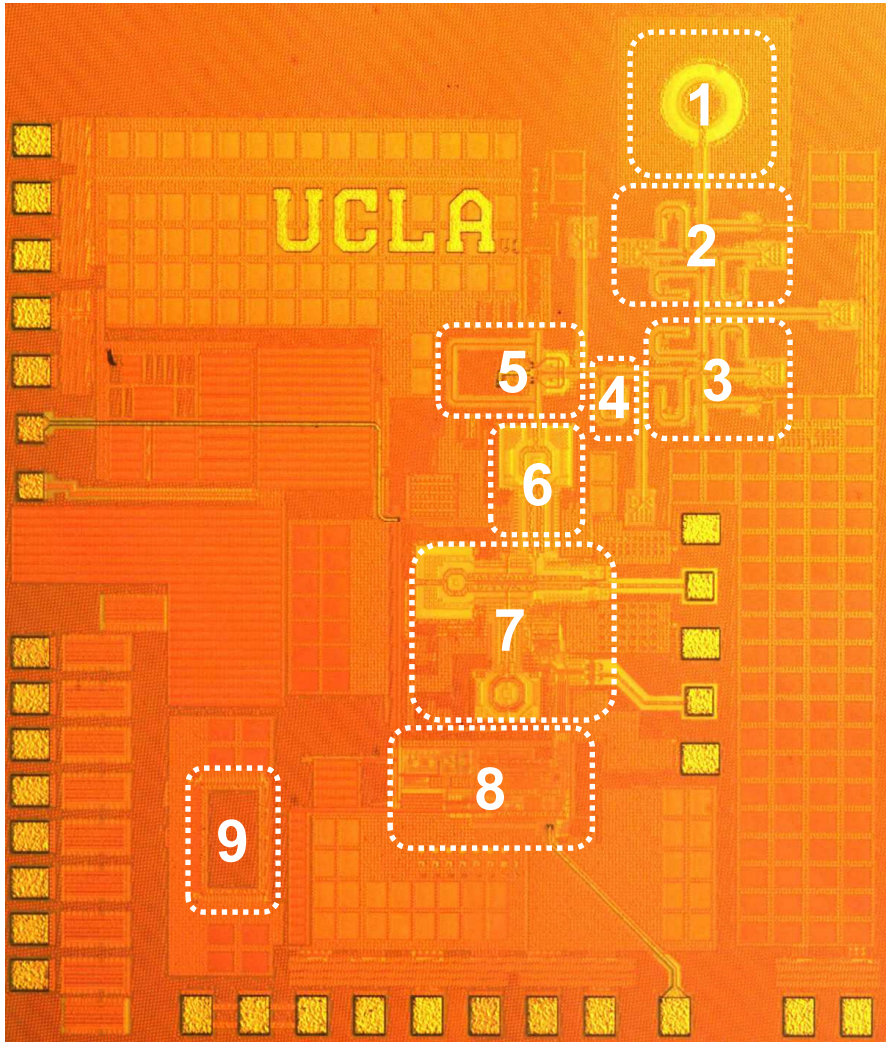
Overview of Complete THz PLL Chip



[Chen15] Z.-Z. Chen et al., "A Wide-band 65nm CMOS 28-34 GHz Synthesizer Module Enabling Low Power Heterodyne Spectrometers for Planetary Exploration," *IEEE Int. Microwave Symp.*, May 2015.

0.56 Terahertz PLL Die Photo

- TSMC Standard 65nm CMOS

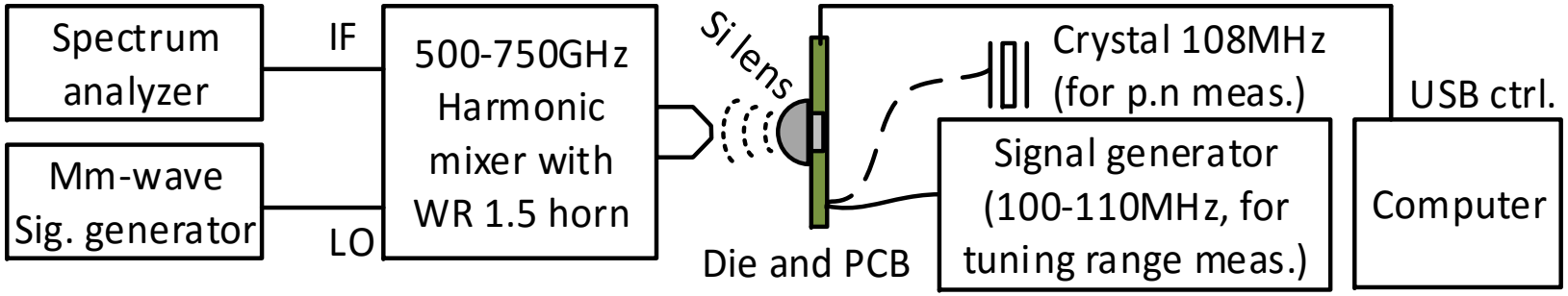


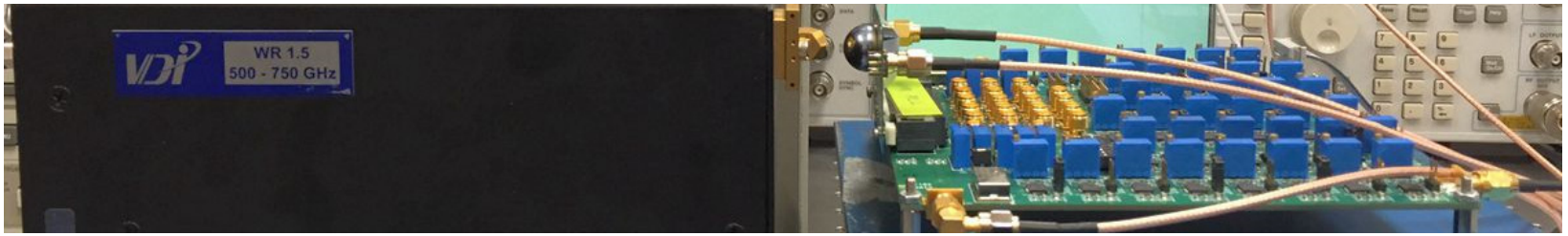
1. On-chip antenna (for testing only)
2. Primary TPCO
3. Aux. TPCO
4. SECO
5. 1st IJFD
6. 2nd IJFD
7. ÷16 divider chain
8. PLL
9. SPI

Die Size: 1.55x1.80mm^2

Spectrum Measurement Setup

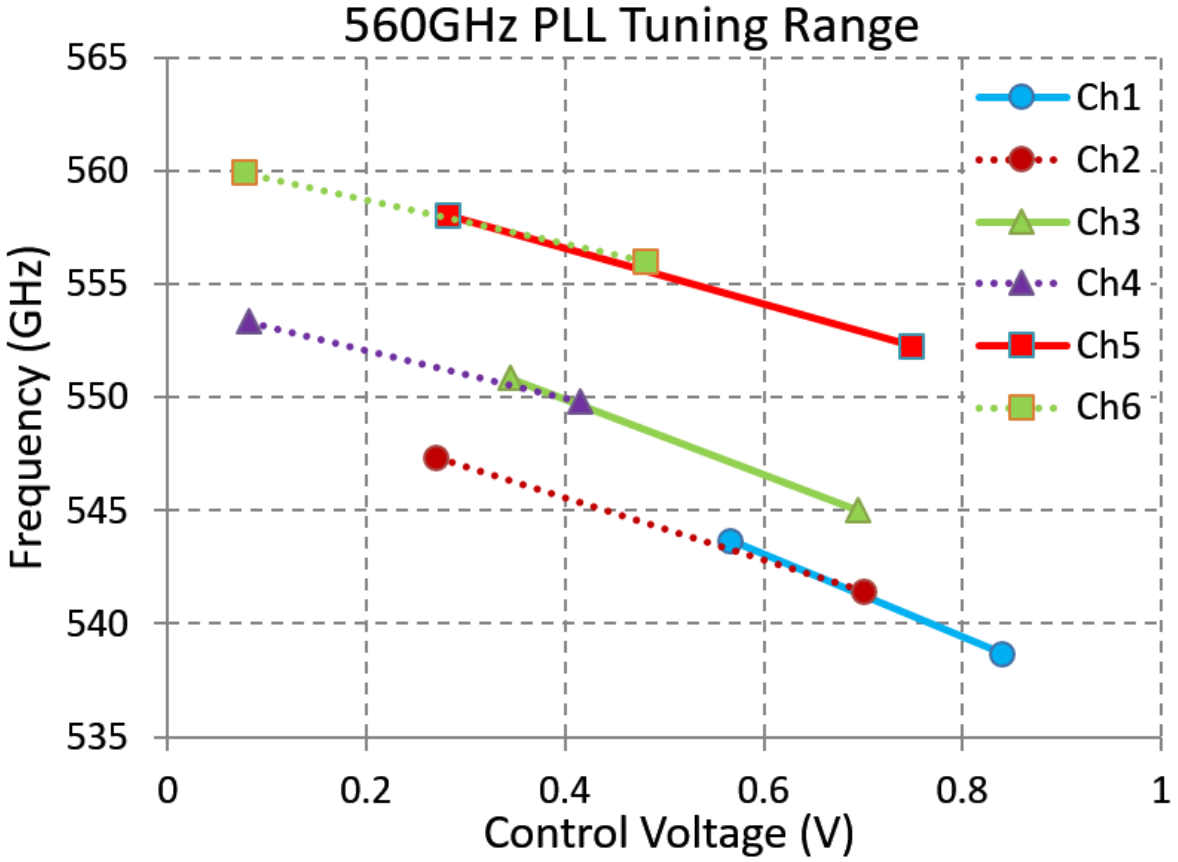
- Focusing signal radiation by using silicon hyper-hemispherical lens
- Down-converting Terahertz signal to IF through sub-harmonic mixer via a WR1.5 horn antenna
- Locking range verified by sweeping reference frequency (100-110MHz)
- Phase noise characterized by using 108MHz crystal





Locking Range Verification

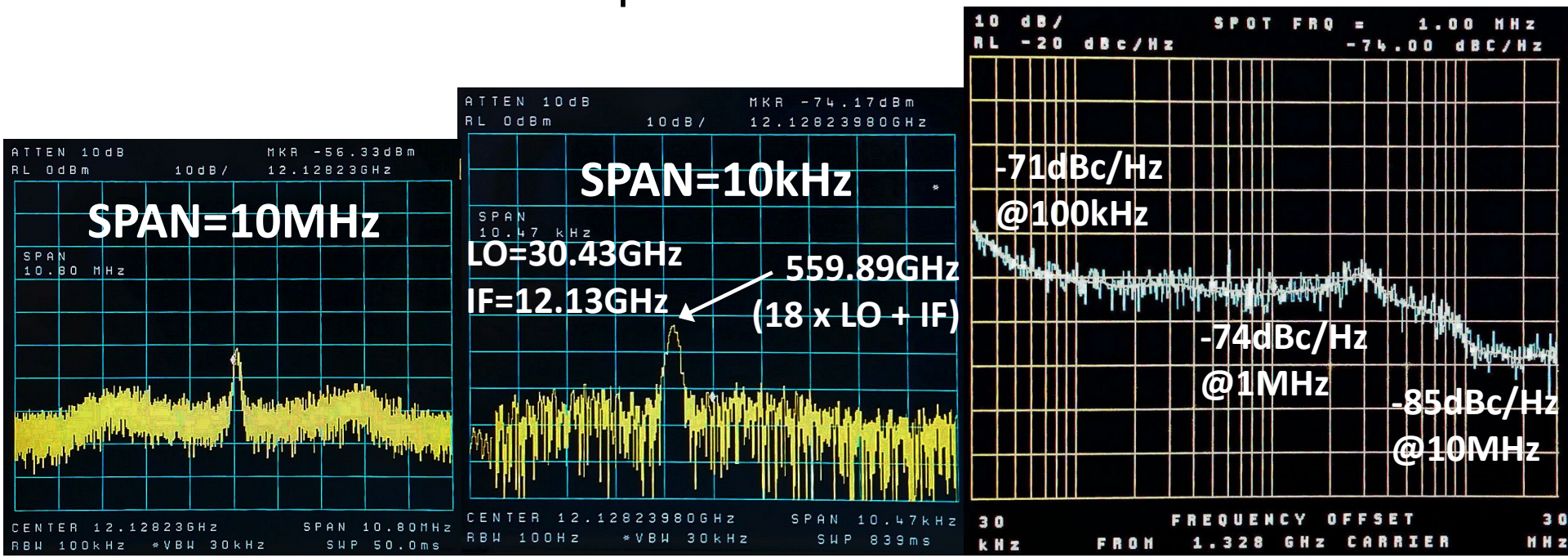
- Locking range verified from 538.67 to 559.89GHz by sweeping reference frequency from 103.9 to 108MHz
- Both DiCAD and inductor switches are configured for achieving above tuning range



	Vsw1 (V)	Vsw2 (V)	D[4:0] (bin)
Ch 1	0.00	1.66	10011
Ch 2	0.00	1.66	10010
Ch 3	0.21	1.69	10001
Ch 4	0.21	1.69	10000
Ch 5	0.66	1.91	01111
Ch 6	0.66	1.91	01110

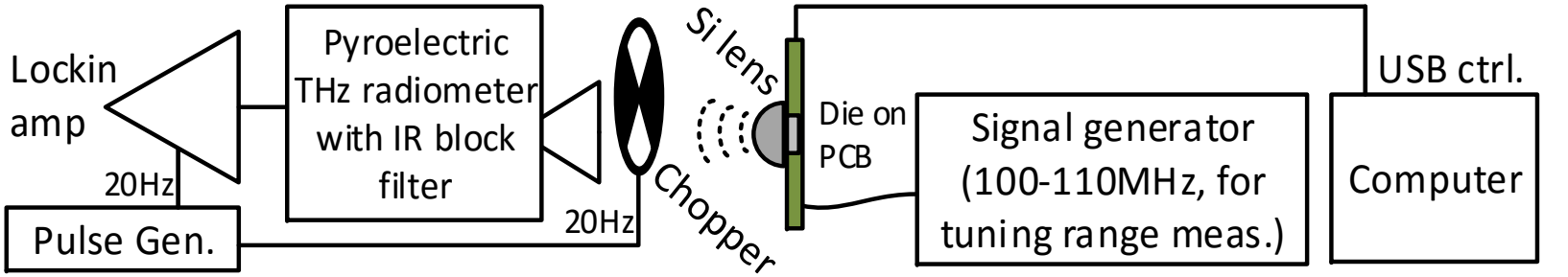
Phase Noise Testing

- Locked Terahertz output is validated by spectrum analyzer with very tight frequency span (10MHz, 10kHz)
- Output frequency is calculated based on LO harmonic number and IF from down-converter output
- Phase noise is characterized by measuring IF tone from down-converter output



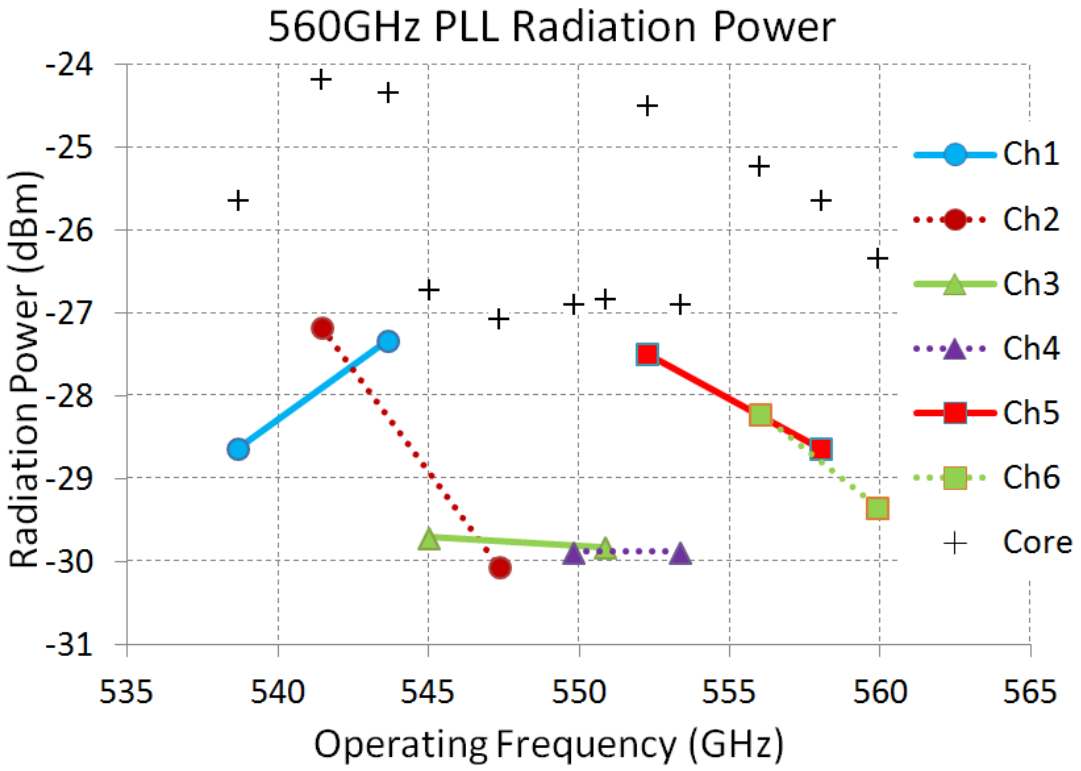
Pout Measurement

- Measuring radiation power with a calibrated pyroelectric THz radiometer.
- Assisted with lock-in amplifier and optical chopper running at recommended chopping frequency
- IR blocking filter is used to reject the thermal radiation from the die

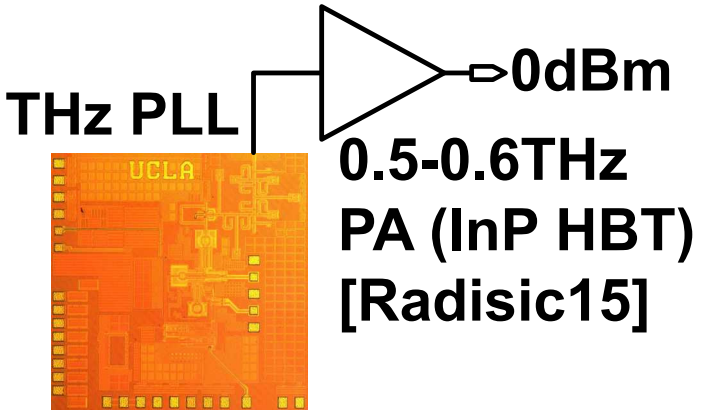


Output Power Measurement Results

- The measured radiated power varies from -30 to -27dBm over the whole locking range.
- 50% Simulated on-chip antenna radiation efficiency suggesting 3dB more output power from the core.



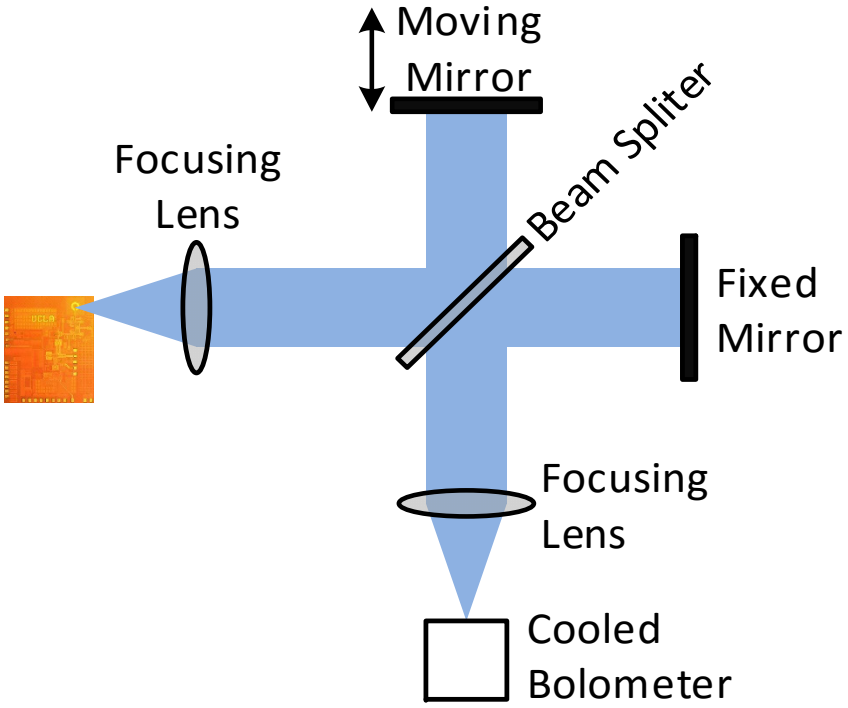
Future solution for high LO power:

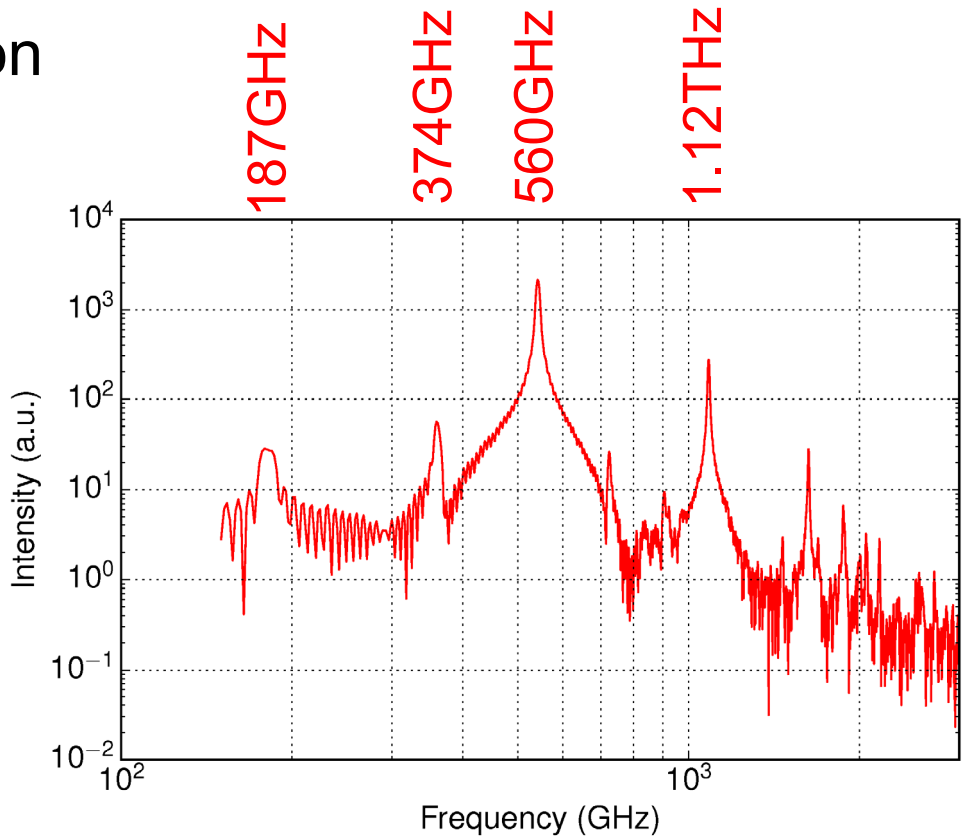


[Radisic15] V. Radisic et al., "InP HBT Transferred Substrate Amplifiers Operating to 600 GHz," IEEE Int. Microwave Symp., May 2015.

Fundamental and Harmonics Leakage Measurement

- Complete radiation spectrum is profiled with FTIR (Fourier transform infrared spectroscopy) system
- 20dB fundamental rejection
- 15dB 2nd harmonic rejection
- 10dB 6th harmonic rejection





Performance Comparison

	Configuration	Max. Freq. (GHz)	Tech. (fmax)	P. N. dBc/Hz @1MHz	PDC (mW)
[1] ISSCC 2014	PLL + VCO	280.0-303.4	SiGe (315GHz)	-82.5	376
[2] ISSCC 2015	PLL + Osc. array	317	SiGe (280GHz)	-79	610
[3] JSSC 2014	VCO + tripler	539.6-561.5	40nm CMOS	Free running	16.8
[4] ISSCC 2014	Non coherent osc. array	519-536 ††	SiGe (500GHz)	Free running	2500
[5] IMS 2015	Coherent VCO array	540-550	65nm CMOS (240GHz)	Free running	1300
[6] JSSC 2015	Injection lock. Osc. chain	485.1-510.7	SiGe (350GHz)	Free running	425
This work	PLL + VCO	538.7-559.9	65nm CMOS (240GHz)	-74	172

Conclusion

- Realized a 0.54-0.56THz frequency synthesizer in 65nm CMOS technology with
  - ✓ 21GHz locking range and -74dBc/Hz phase noise at 1MHz offset
  - ✓ -27dBm power radiated into space (-24dBm on-chip output power)
  - ✓ 172mW power consumption from 1V supply

- Significantly reduced weight, size and power of the LO chain in existing NASA JPL Terahertz instrument (2.5kg, 3000cm^3, 11.5W)

Acknowledgements

This work is supported by

US AFOSR under Grant No. FA9550-12-1-0181
and
US ARO under Grant No. W911NF-14-1-0665.

Thanks for your attention!

A Scalable 28GHz Coupled-PLL in 65nm CMOS with Single-Wire Synchronization for Large-Scale 5G mm-Wave Arrays

Abhishek Agrawal, Arun Natarajan

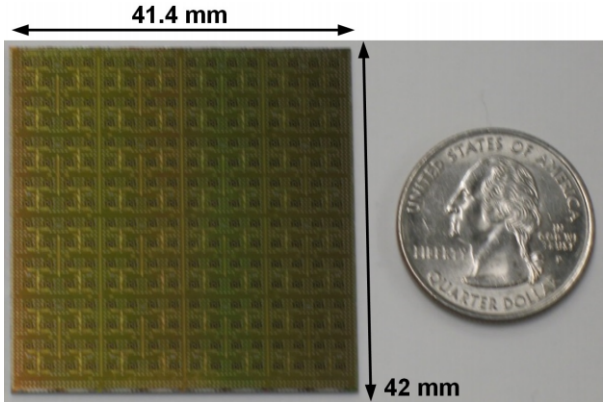
Oregon State UNIVERSITY OSU

Outline

- **Motivation**
- Noise and Stability in Coupled-PLLs
- 28GHz Bidirectional Coupled-PLL in 65nm CMOS
- Measured Performance
- Conclusion and Future Work

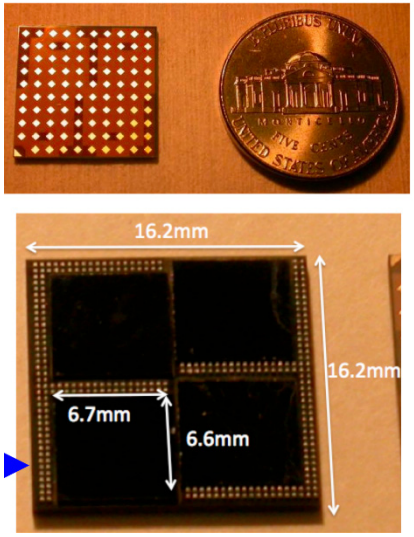
Scalable Arrays

256-element 60GHz array



[Zihir et al., RFIC 2015]

64-element 94GHz array



[Valdes-Garcia et al., RFIC 2013]

100-element 2.6GHz MIMO array

[J. Vieira et al., Globecom 2014]

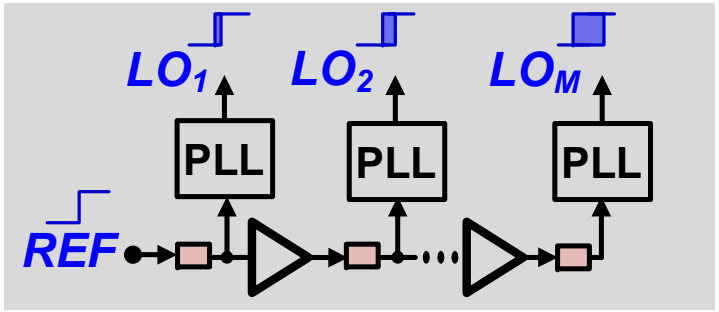
- Scalable arrays based on tiled unit-cells demonstrated at 60GHz and 94GHz.
- Scalability for large-scale arrays requires:
  - scalable RF interface to antennas,
  - scalable IF signal combining/distribution, and,
  - scalable synchronization between unit cells.

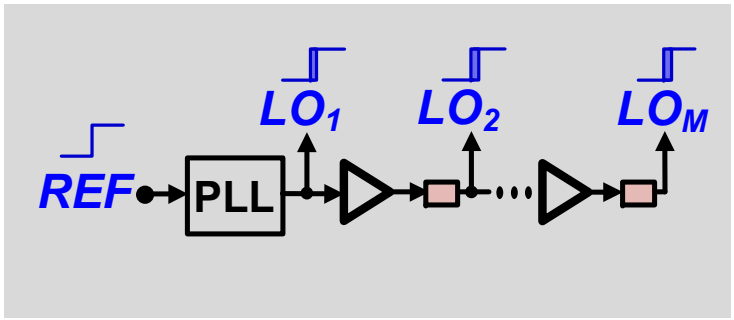
Clock Distribution Approach

REF Distribution

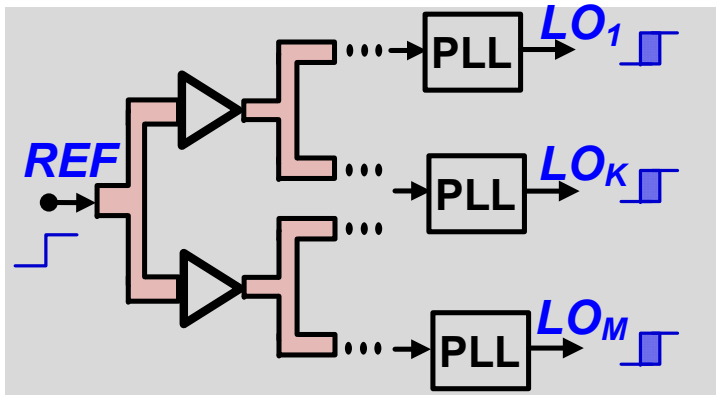
LO Distribution

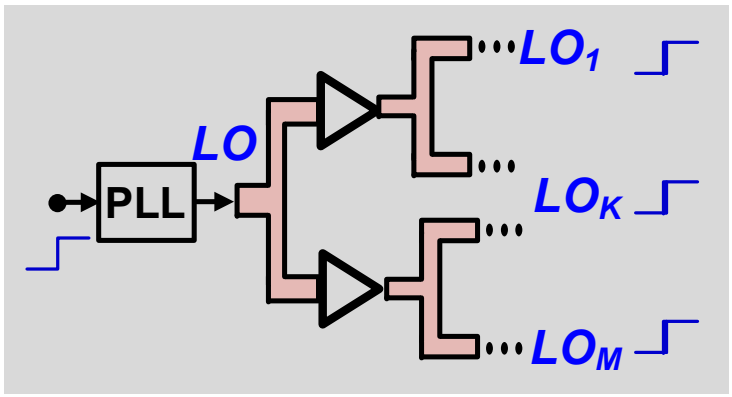
Daisy Chain





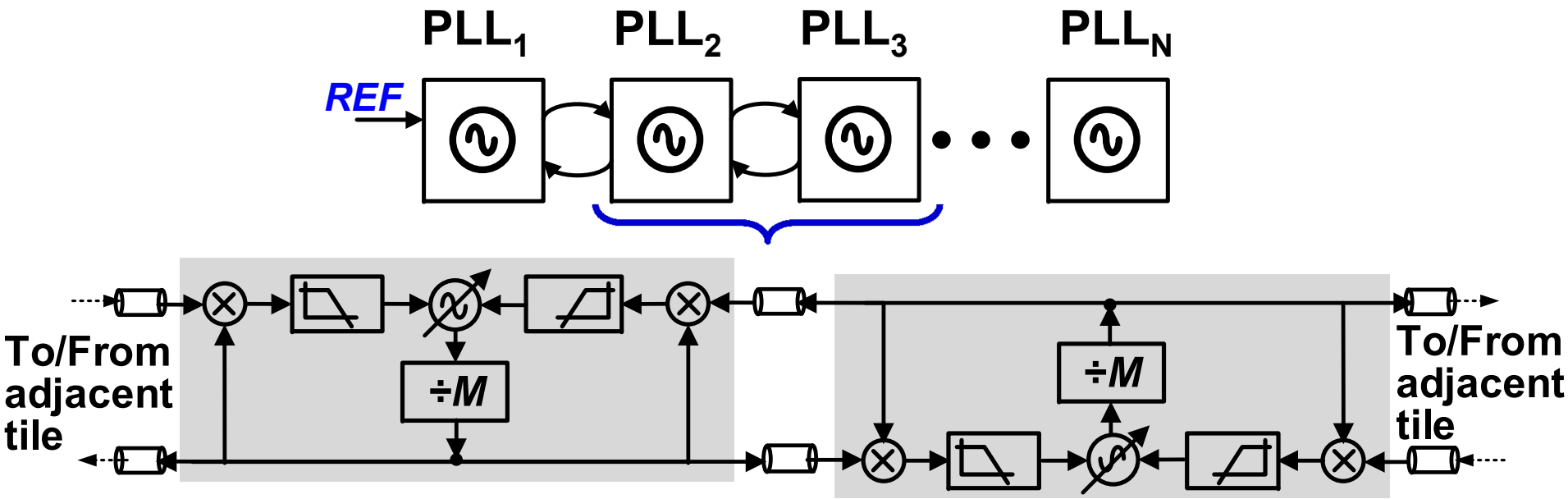
H-Tree





	Scalability	Phase Drift/Skew	Phase Noise
REF Daisy-Chain	✓✓✓	×××	×××
REF H-Tree	✓✓	×	××
LO Daisy-Chain	✓	××	×
LO H-Tree	×××	✓✓	✓✓

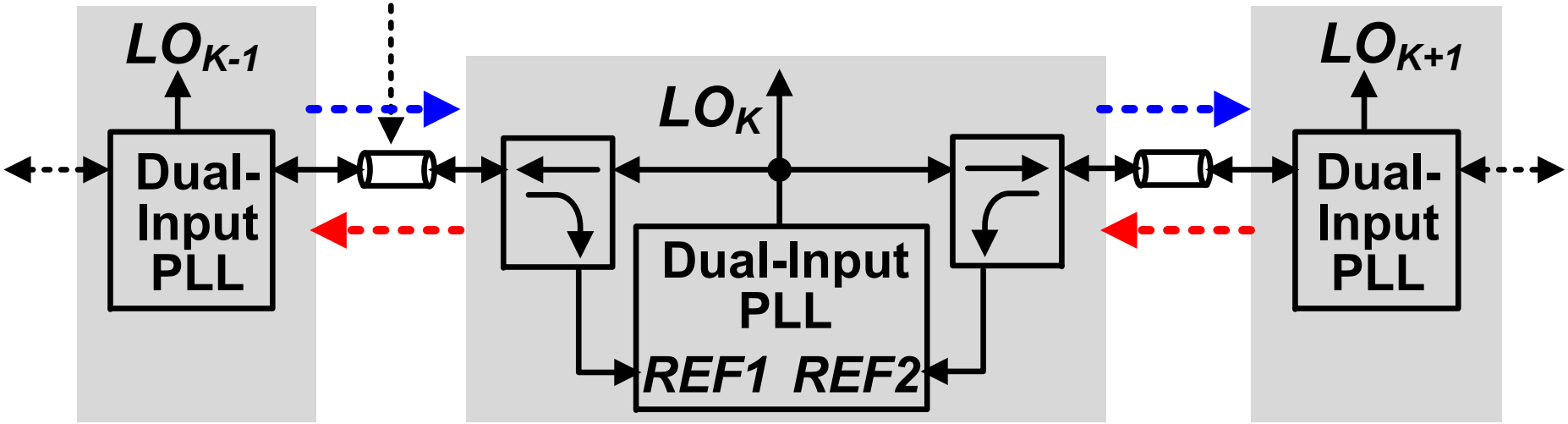
Bidirectional Clock Distribution



- ✓ Coherent clock generation.
- ✓ Phase noise reduction by *N* (within coupling bandwidth).
- ✗ Doubles the number of IO pins.

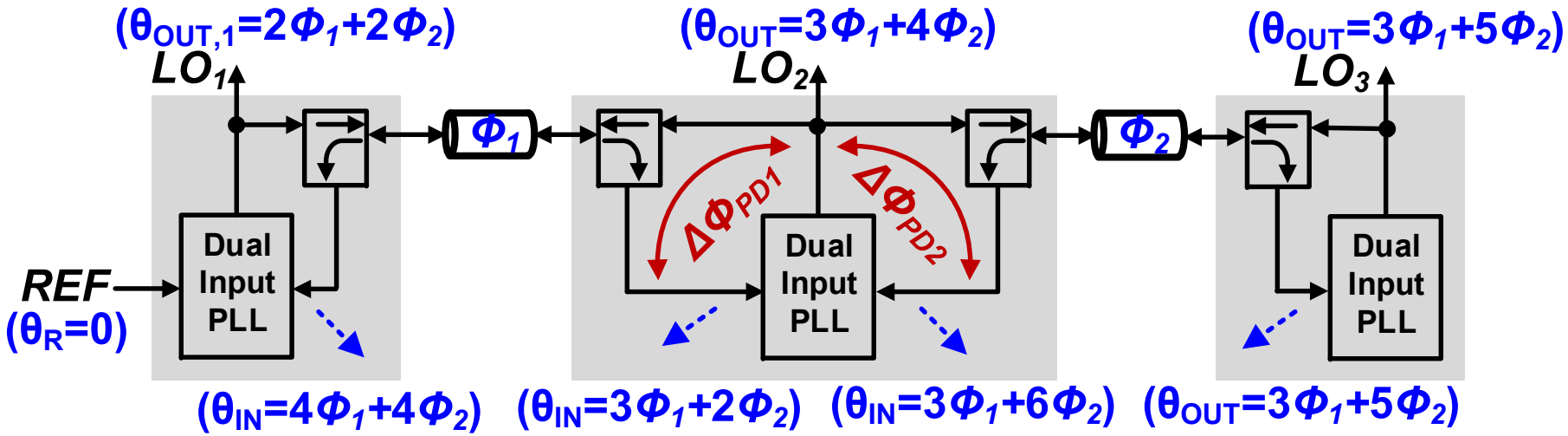
Single-wire Bidirectional Coupling

Single-wire coupling



- ✓ Simplicity of daisy-chain distribution - scalable approach due to single wire coupling.
- ✓ Lower phase noise (factor of *N* improvement).

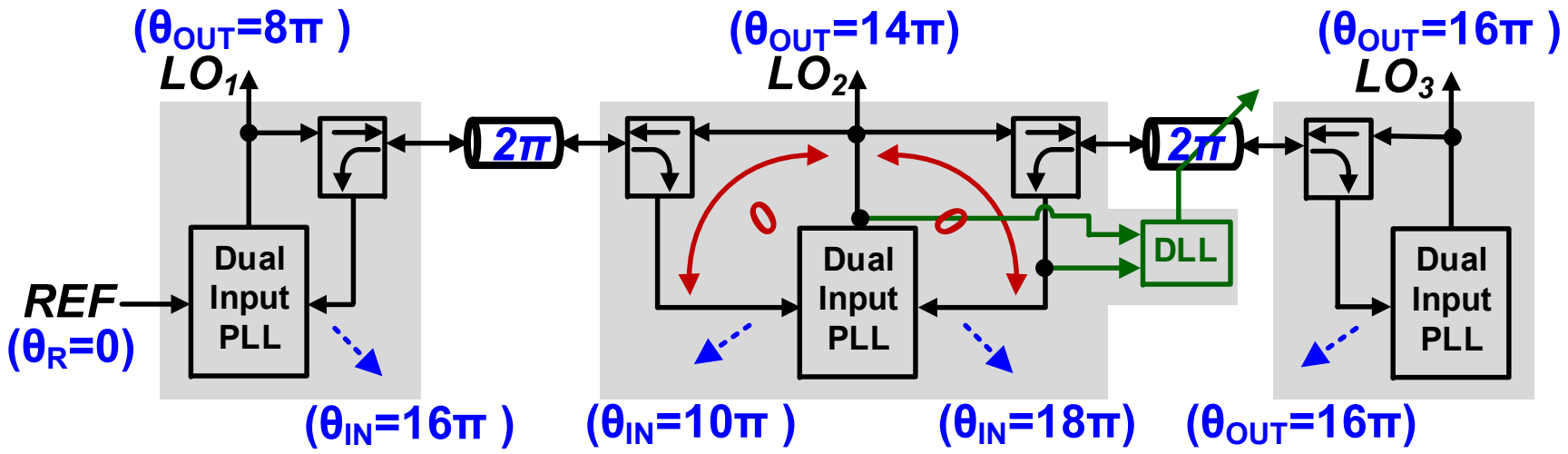
Clock Phase Skew due to Interconnect



$$\text{Type 2 PLL} \Rightarrow \Delta\Phi_{PD1} = -\Delta\Phi_{PD2}$$

- Minimize phase offset to improve PLL locking and noise.
- Phase offset removed if interconnect phase shift is multiple of 2π.

Removing Clock Skew



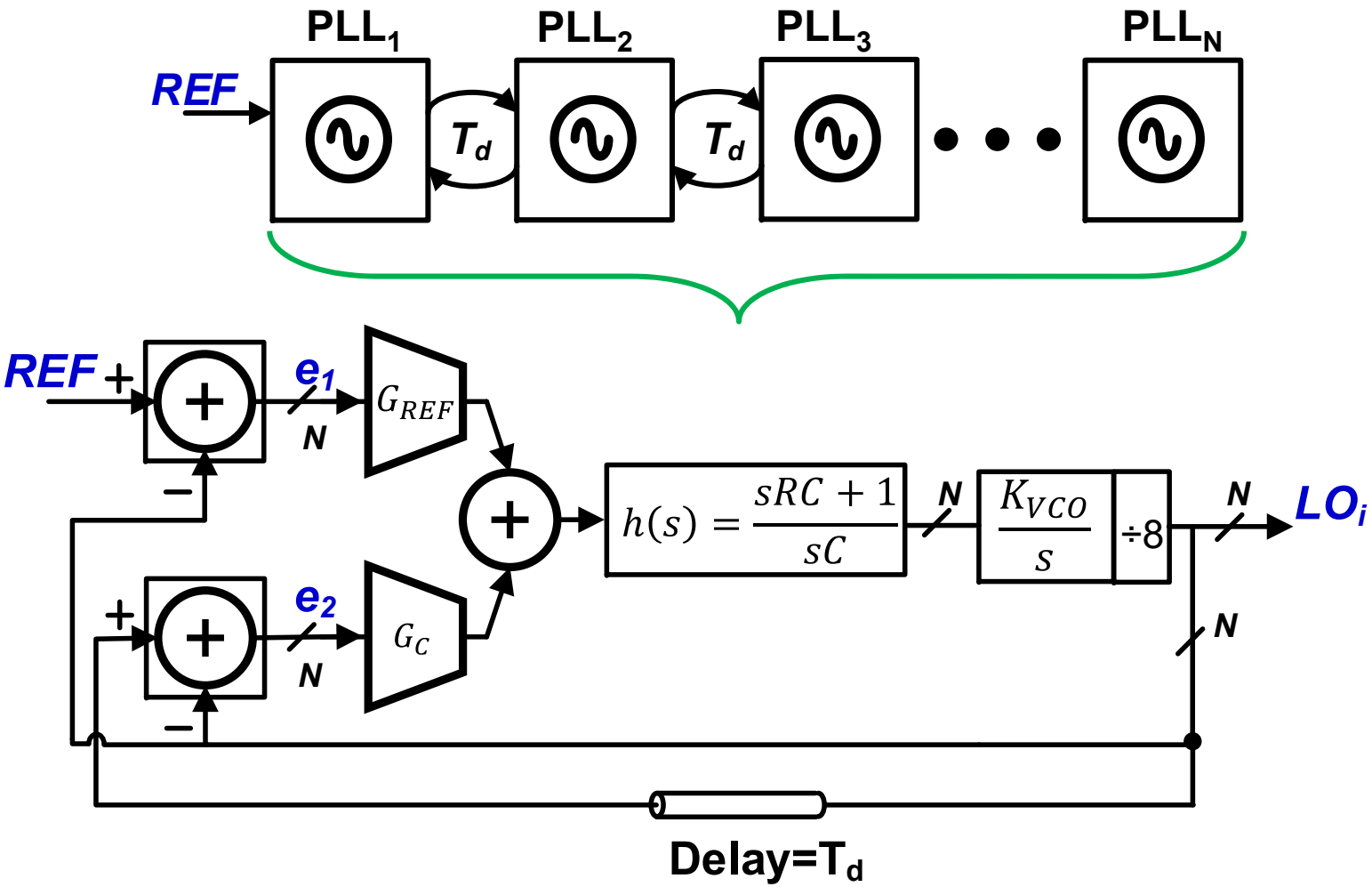
$$\Delta\Phi_{PD1} = \Delta\Phi_{PD2} = 2k\pi$$

- DLL controls variable phase shift in clock signal distribution path to lower phase offset for dual-input PLL.

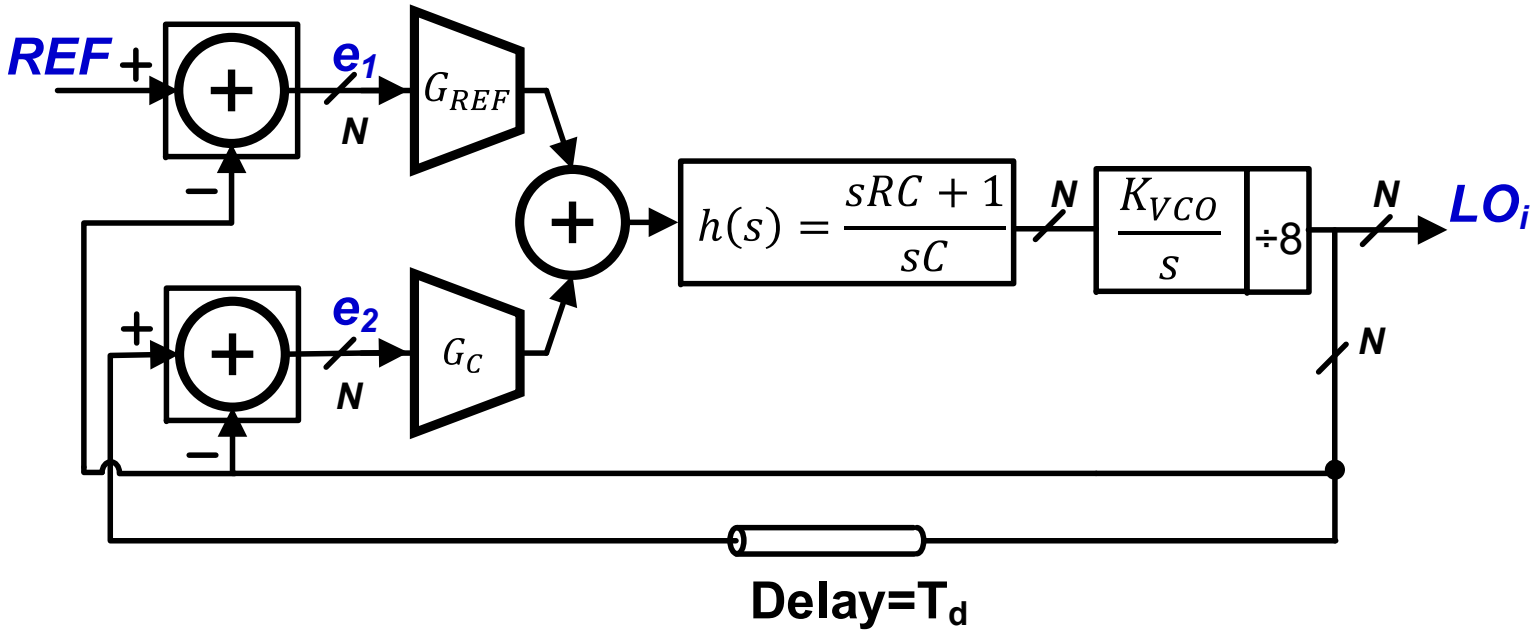
Outline

- Motivation
- **Noise and Stability in Coupled-PLLs**
- 28GHz Bidirectional Coupled-PLL in 65nm CMOS
- Measured Performance
- Conclusion and Future Work

Coupled PLL: Generalized Model

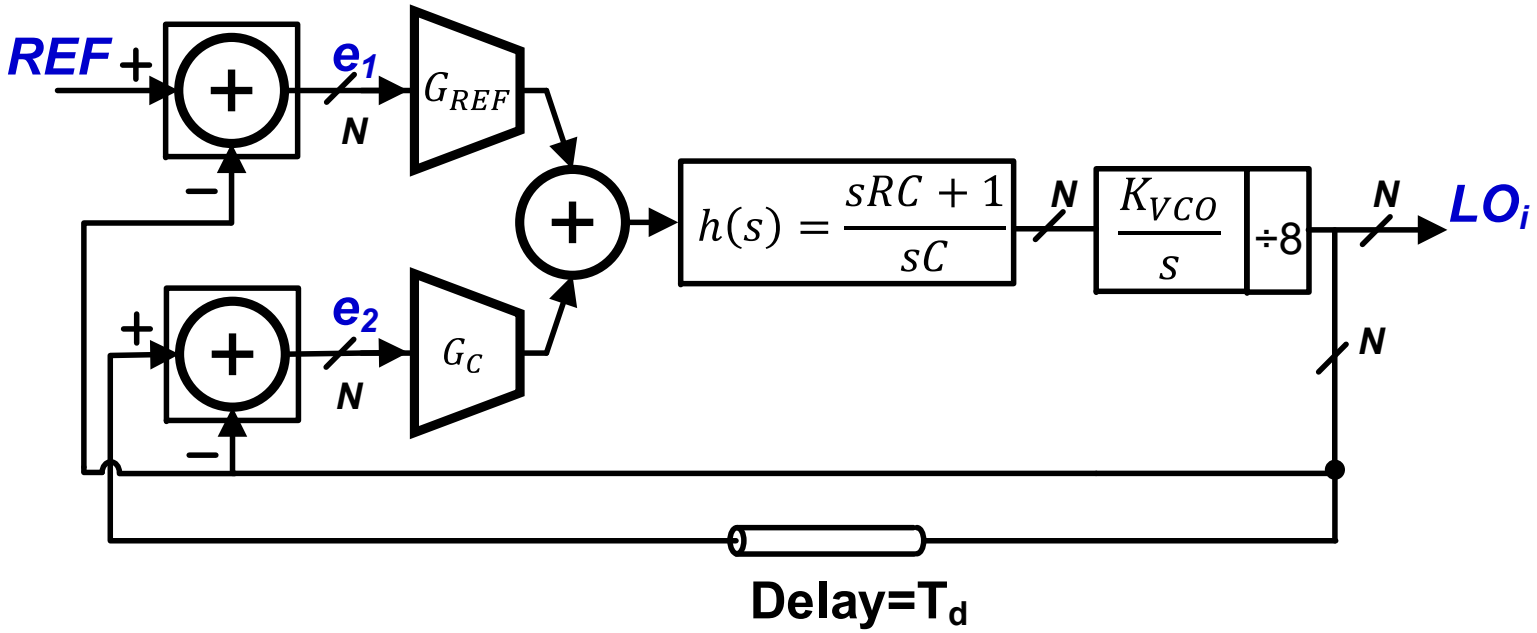


Coupled PLL: Noise Transfer Function



- For reference loop: $\omega_{UGB,REF} = G_{REF} R K_{VCO}$
- For coupled loop: $\omega_{UGB,C} = G_C R K_{VCO}$

Coupled PLL: Noise Transfer Function

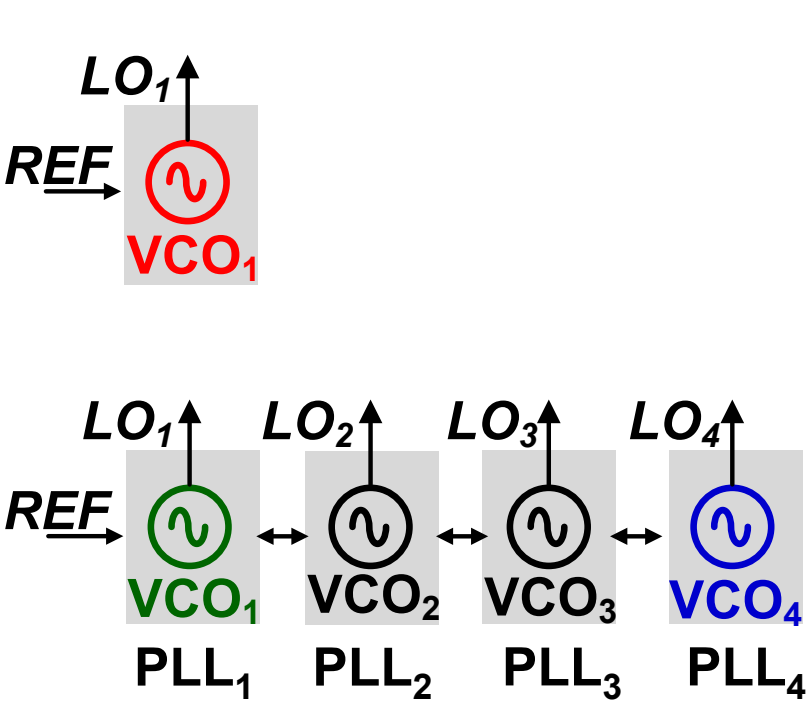


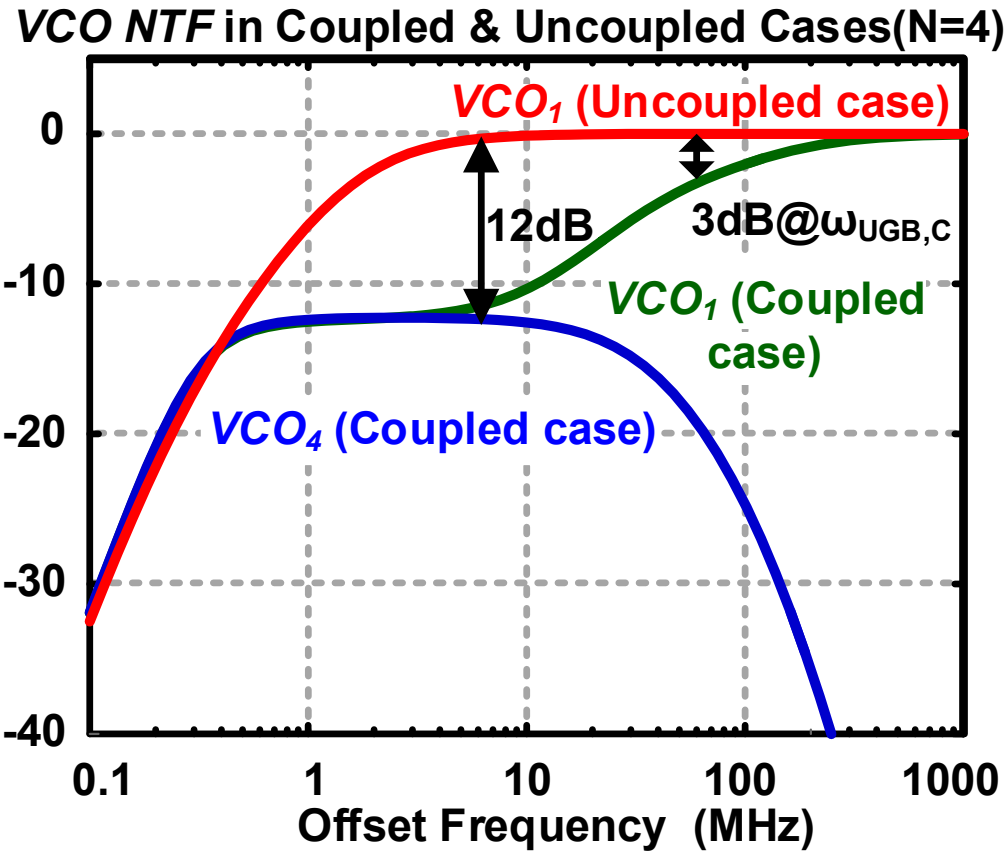
Noise transfer function (*NTF*) for VCO and reference noise:

$$NTF_{VCO} = \left(I - (A_c G_c + A_{r1} G_{REF}) h(s) \frac{K_{VCO}}{s} \right)^{-1}$$

$$NTF_{REF} = \left(I - (A_c G_c + A_{r1} G_{REF}) h(s) \frac{K_{VCO}}{s} \right)^{-1} A_{r2} G_{REF} h(s)$$

VCO Noise Transfer Function

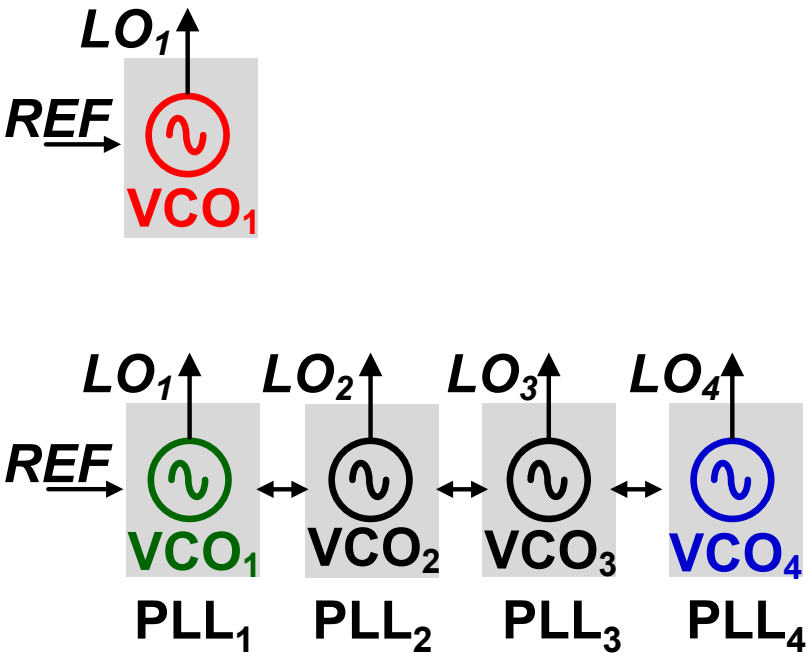


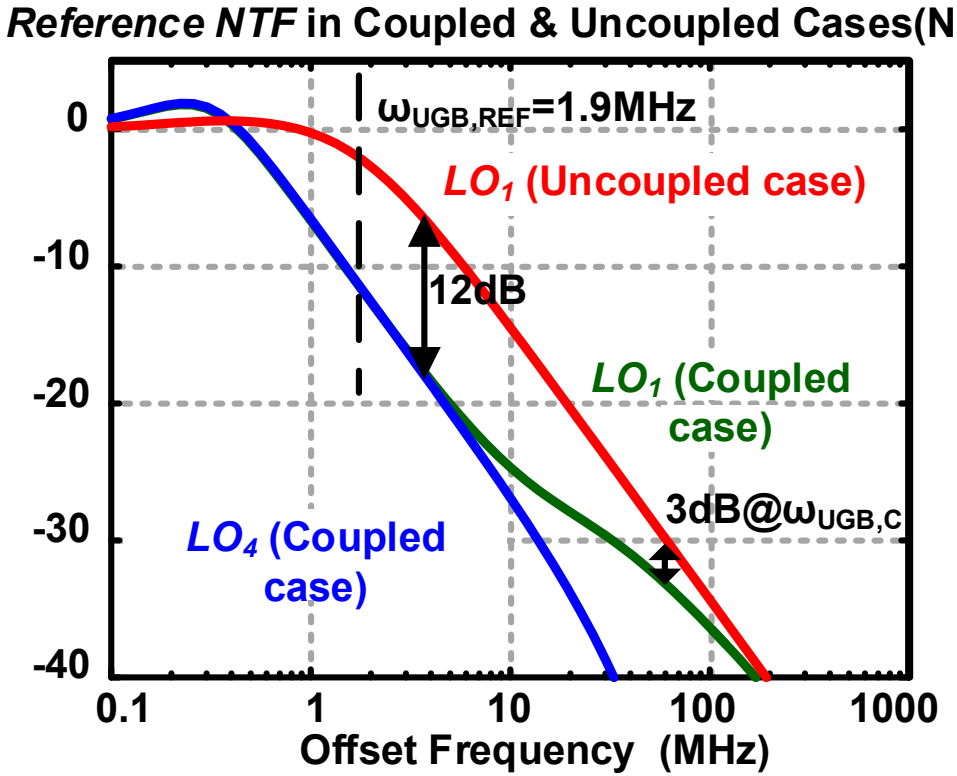


- *NTF* from each VCO to *LO* within coupling bandwidth is -12dB.
- Four VCOs produce four uncorrelated noise sources (add 6dB).

  → **Overall noise reduction -6dB.**

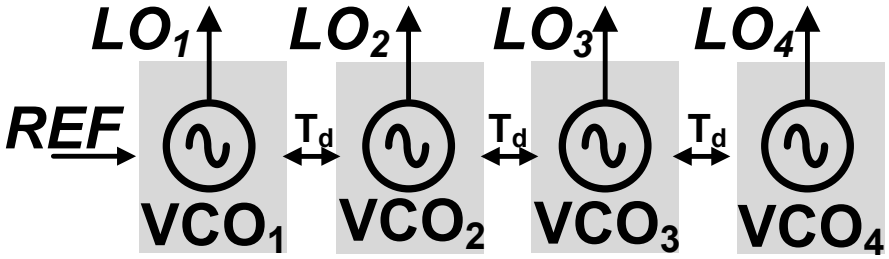
Reference Noise Transfer Function

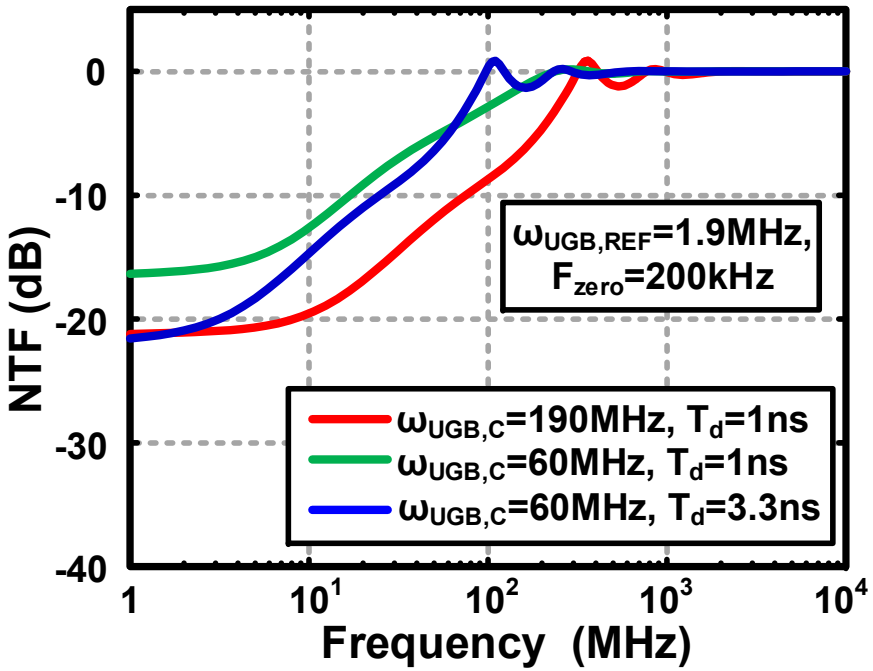


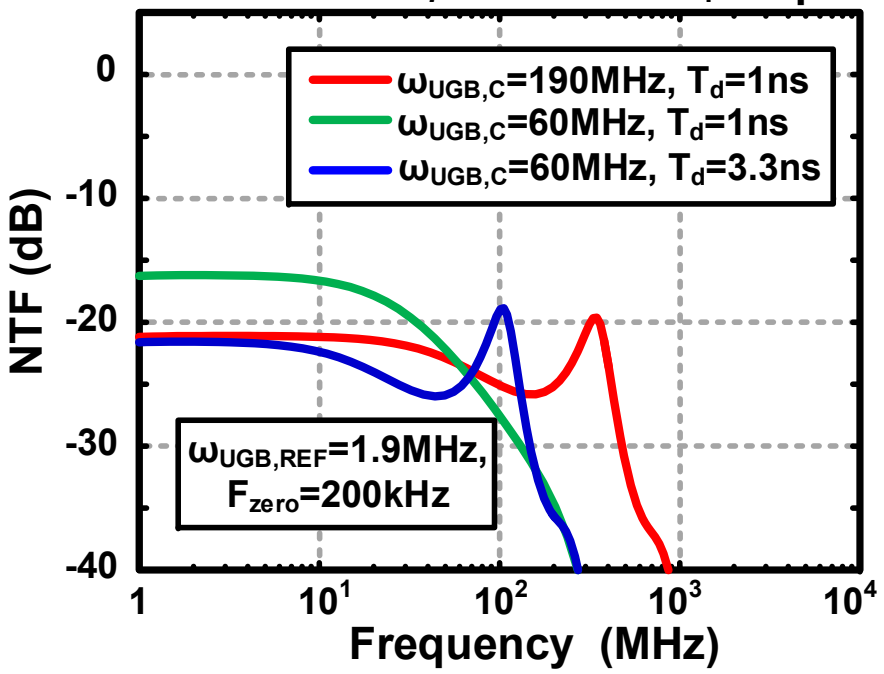


- Reference *NTF* loop bandwidth decreases with increasing *N* if loop parameters kept constant across PLLs.
- Asymmetry in *NTF* since *REF* provided to PLL1.

Effect of Delay on Stability



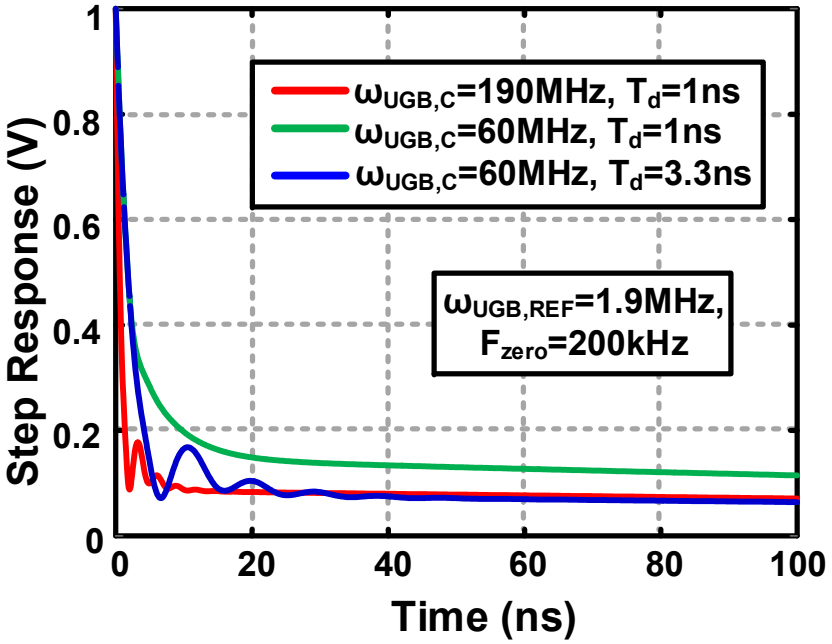




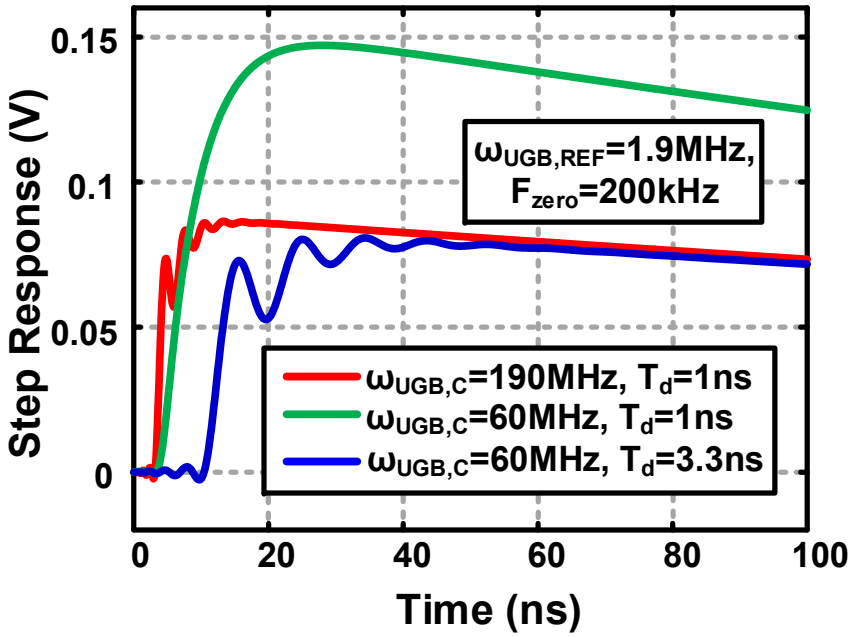
- Higher delay in the coupling path → smaller $\omega_{UGB,C}$ to ensure stability.

Effect of Delay on Stability

Step Response **from** ***VCO$_1$*** **noise to** ***LO$_1$*** **output**



Step Response from ***VCO$_1$*** **noise to** ***LO$_4$*** **output**



- Example: Coupling delays with 1nS (0.3m in air) are feasible with coupling bandwidth of 60MHz.
- Stability analysis can be done by applying generalized Nyquist stability criteria for a MIMO system.

S. Skogestad and I. Postlethwaite,"Multivariable Feedback Control", John Wiley and Sons, 2005

Outline

- Motivation
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- **28GHz Bidirectional Coupled-PLL in 65nm CMOS**
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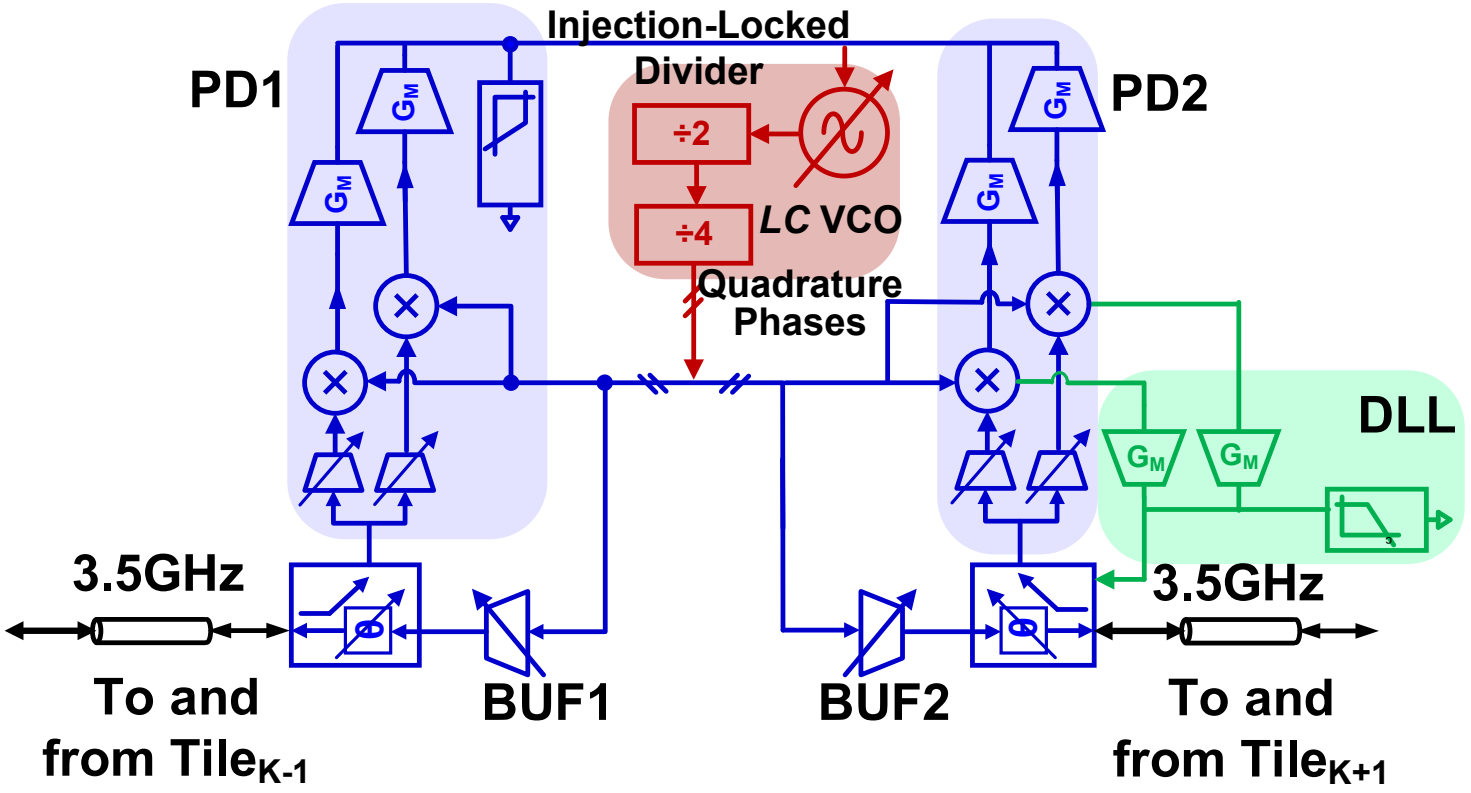
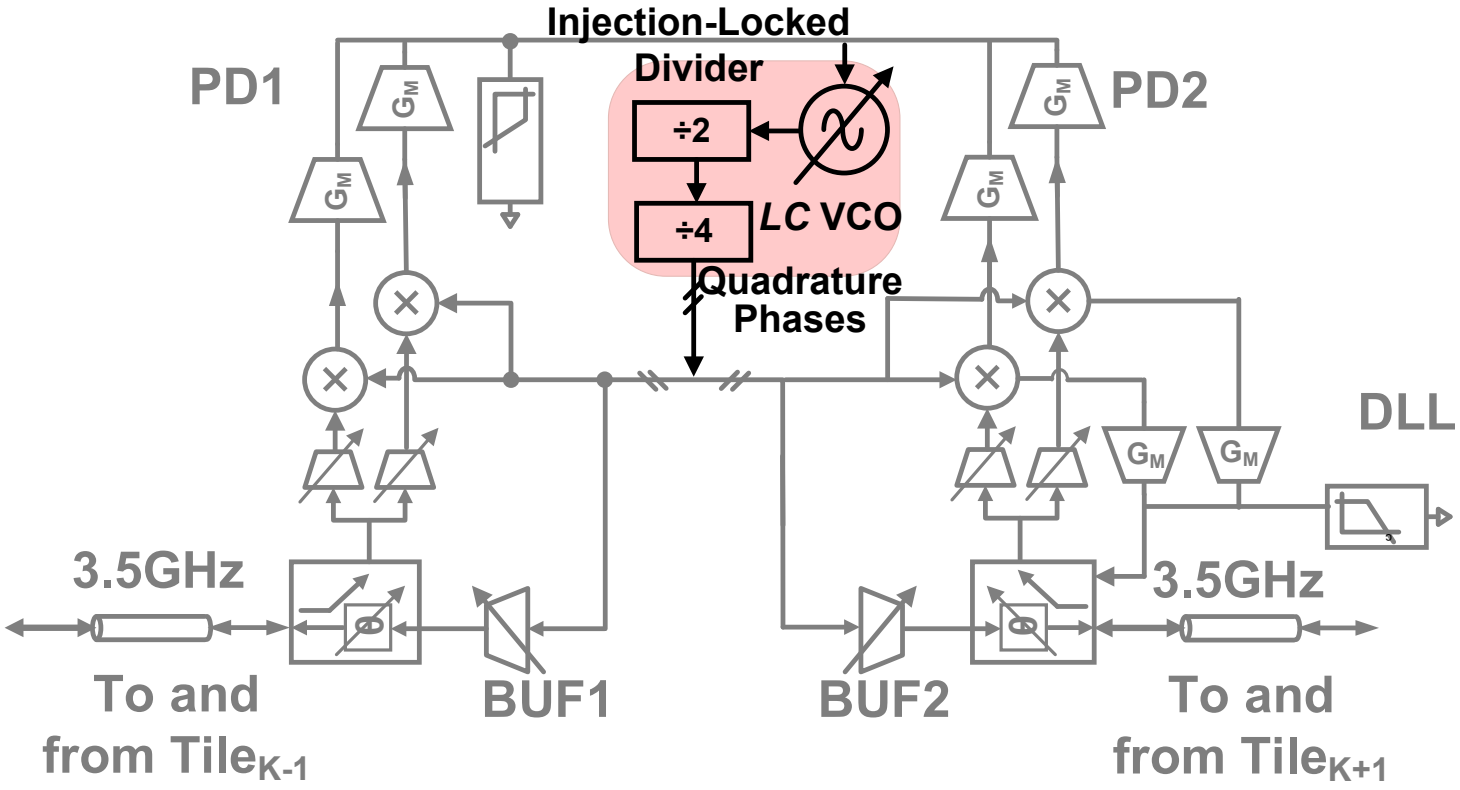
28GHz Dual-Input PLL



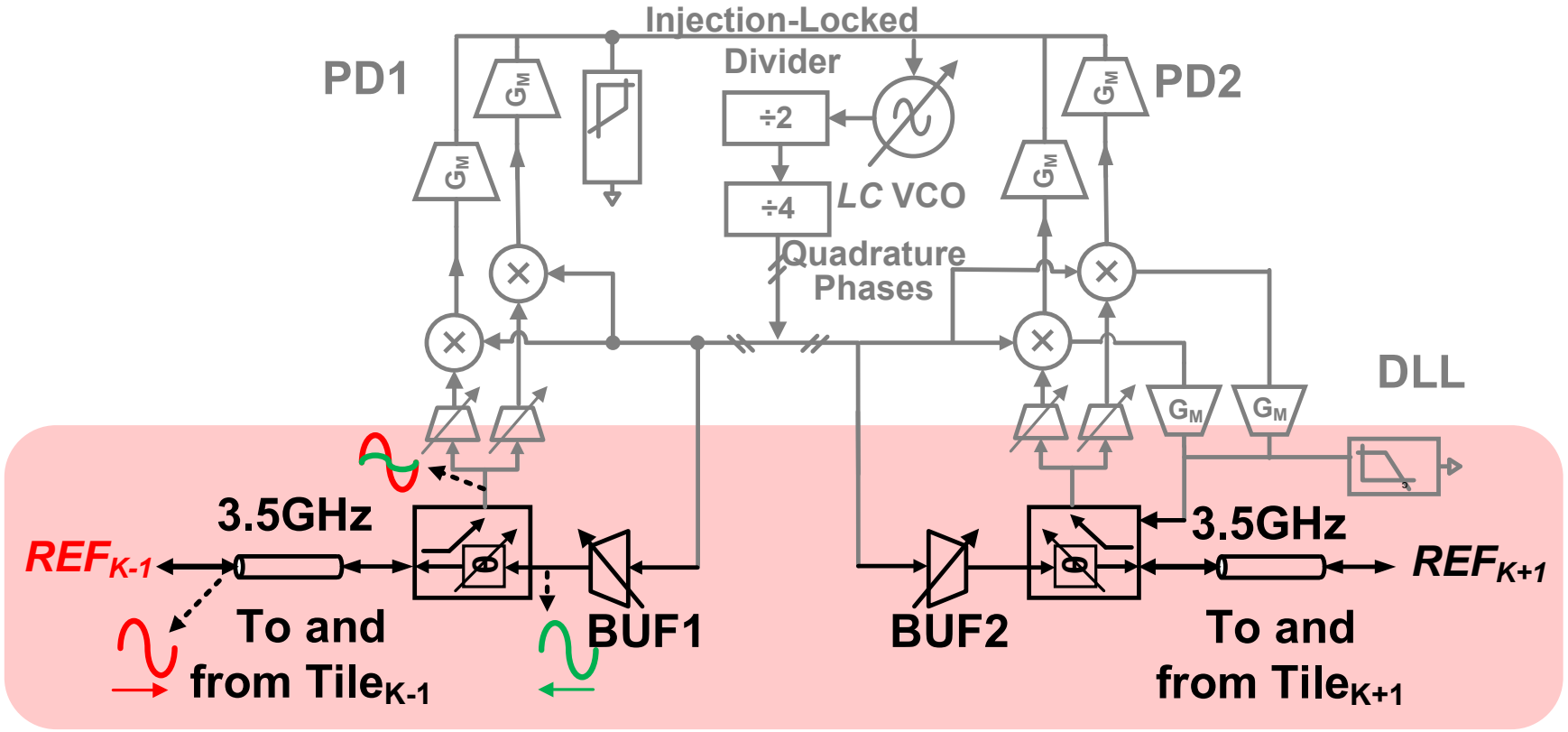
- 28GHz PLL with injection-locked divider and quadrature mixer-PD.
- Coupling using VCO/8: 3.5GHz signal between ICs.
- Variable phase shift for DLL distributed across multiple blocks to provide overall 2π phase shift.

Dual-input 28GHz PLL: VCO & Divider



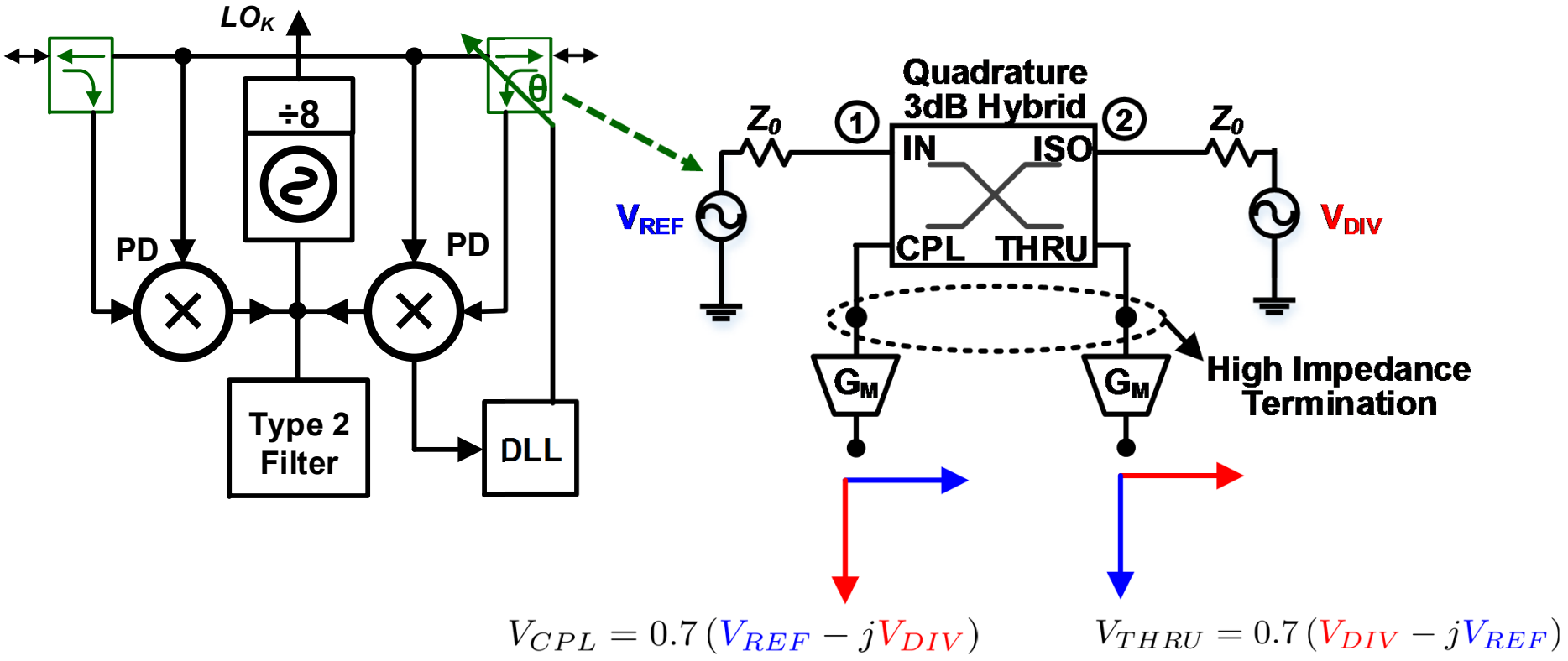
- *LC* VCO → 25.3GHz to 30.4GHz frequency tuning range.
- 25.5GHz to 30.5GHz injection-locked divider.
- CML divider generates ~3.5GHz divided clock from 14GHz input.

28GHz PLL: Single-Wire Coupling Block



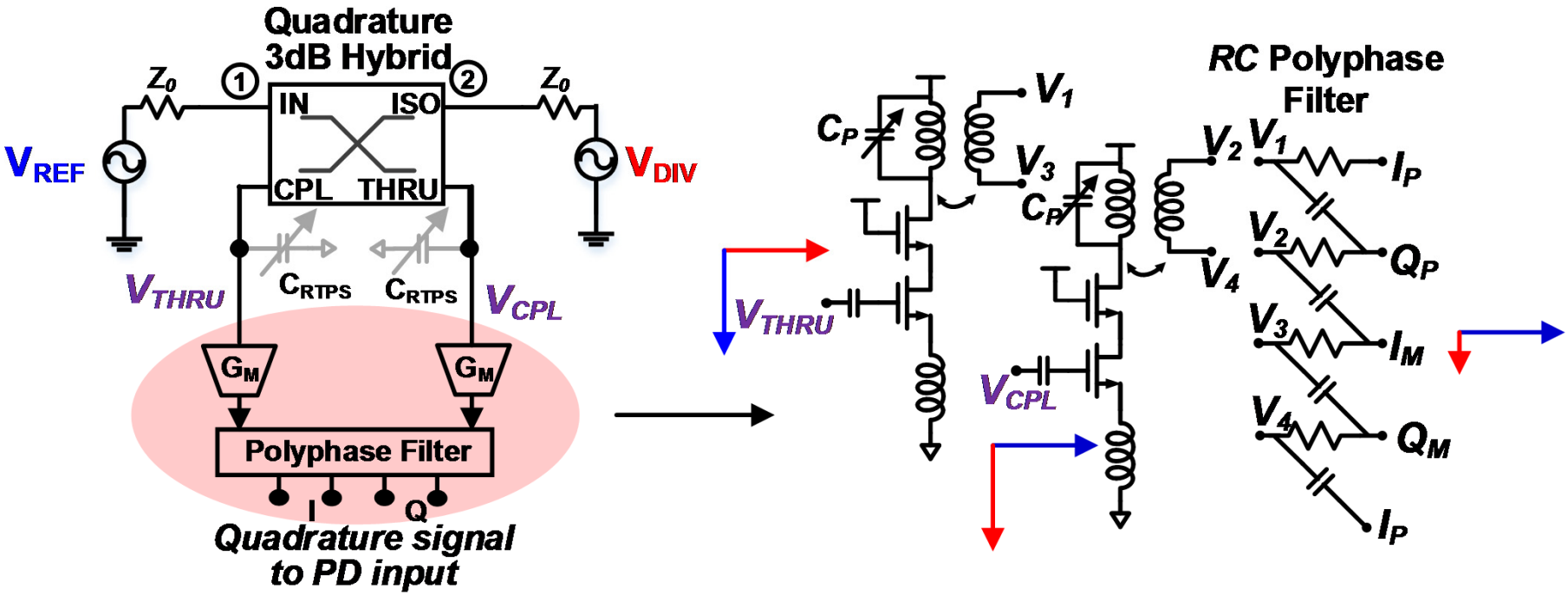
- Input coupling block must distinguish between *REF* input and VCO buffer output on same wire.
- Residual leakage will cause phase offset in Type 2 PLL.

Single-Wire Coupling Block



- Lumped 3.5GHz hybrid coupler implemented using transformer and capacitor.
- V_{REF} **leads** at coupled port & V_{DIV} **leads** at through port.

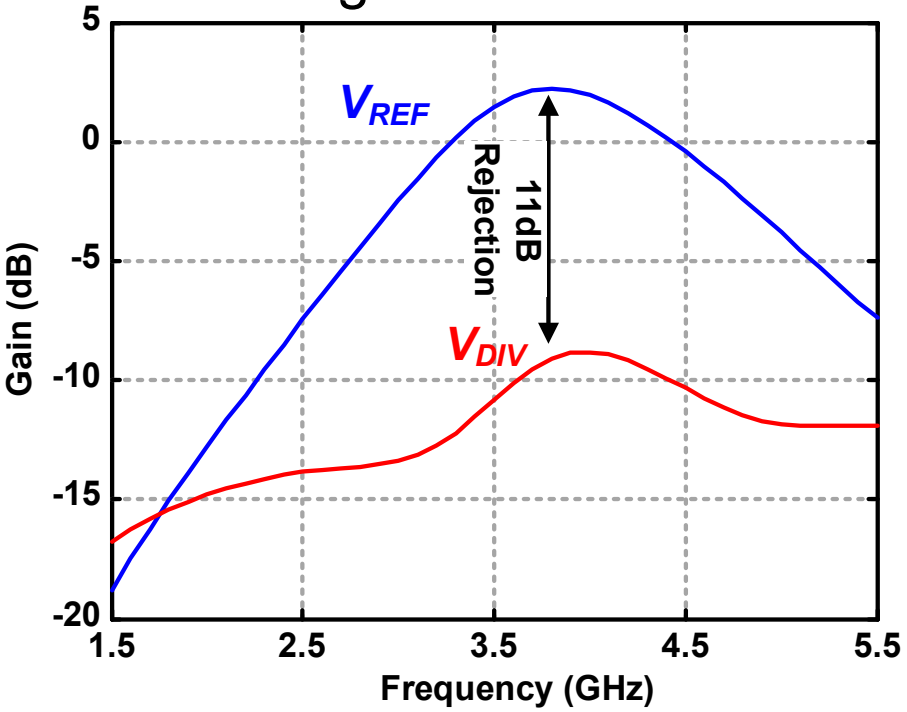
Single Wire-Coupling Block



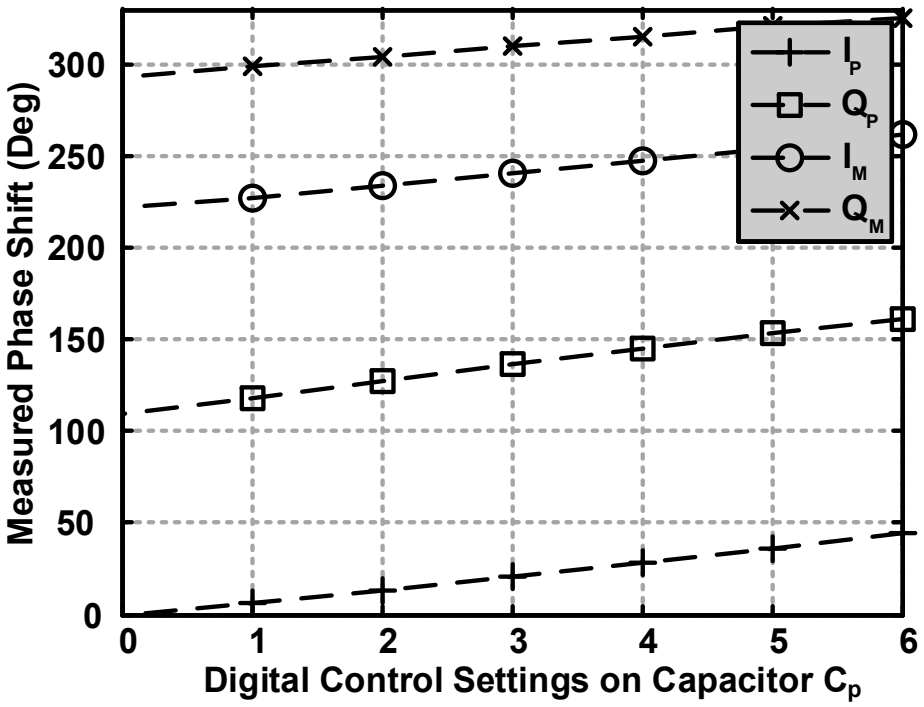
- V_{REF} leads at coupled port & V_{DIV} leads at through port.
- Polyphase filter **rejects** signal due to V_{DIV} at output, selects signal due to V_{REF}.

Single-Wire Coupling Block

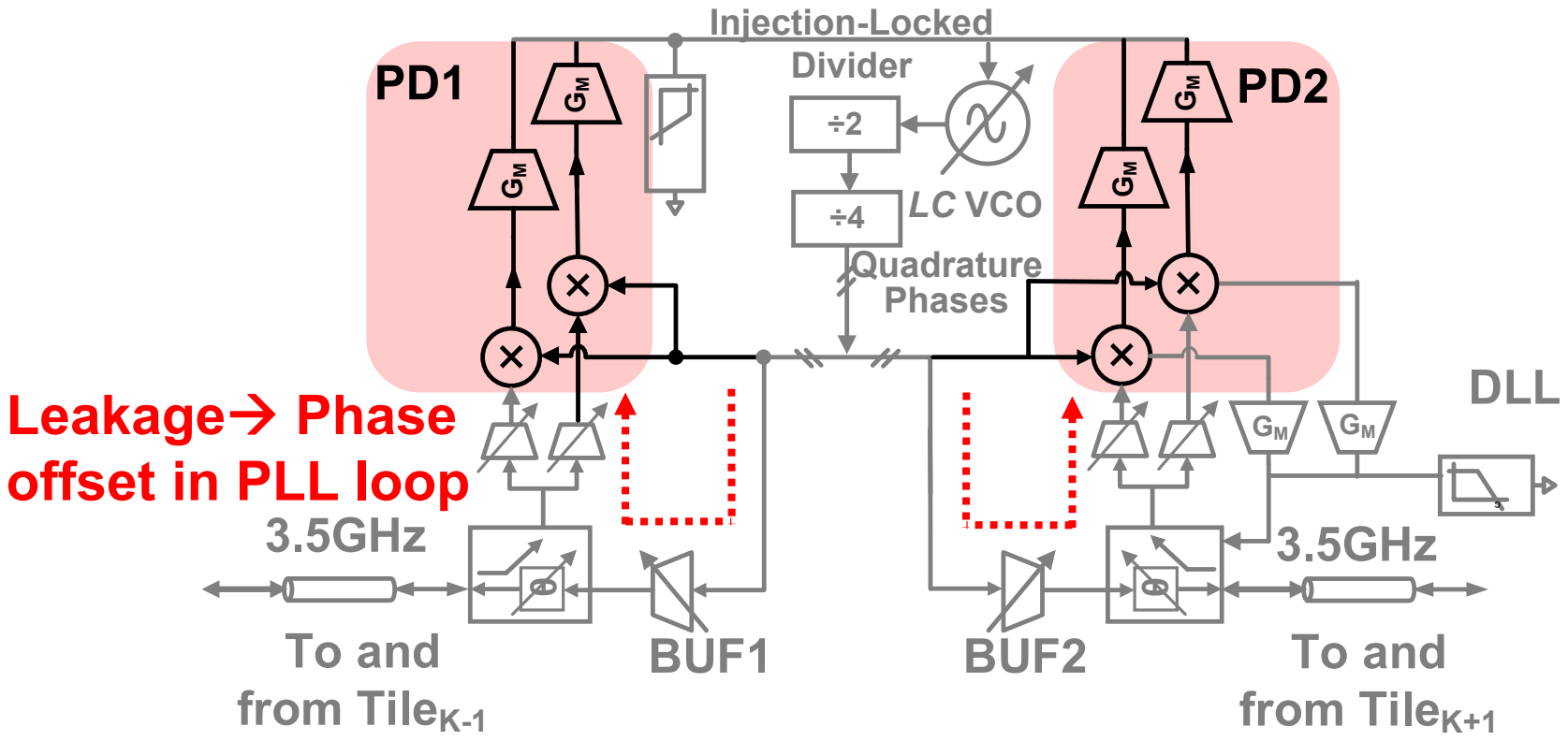
Simulated gain from V_{REF} and V_{DIV} to quadrature output including bond wire.



Measured phase difference between quadrature outputs.

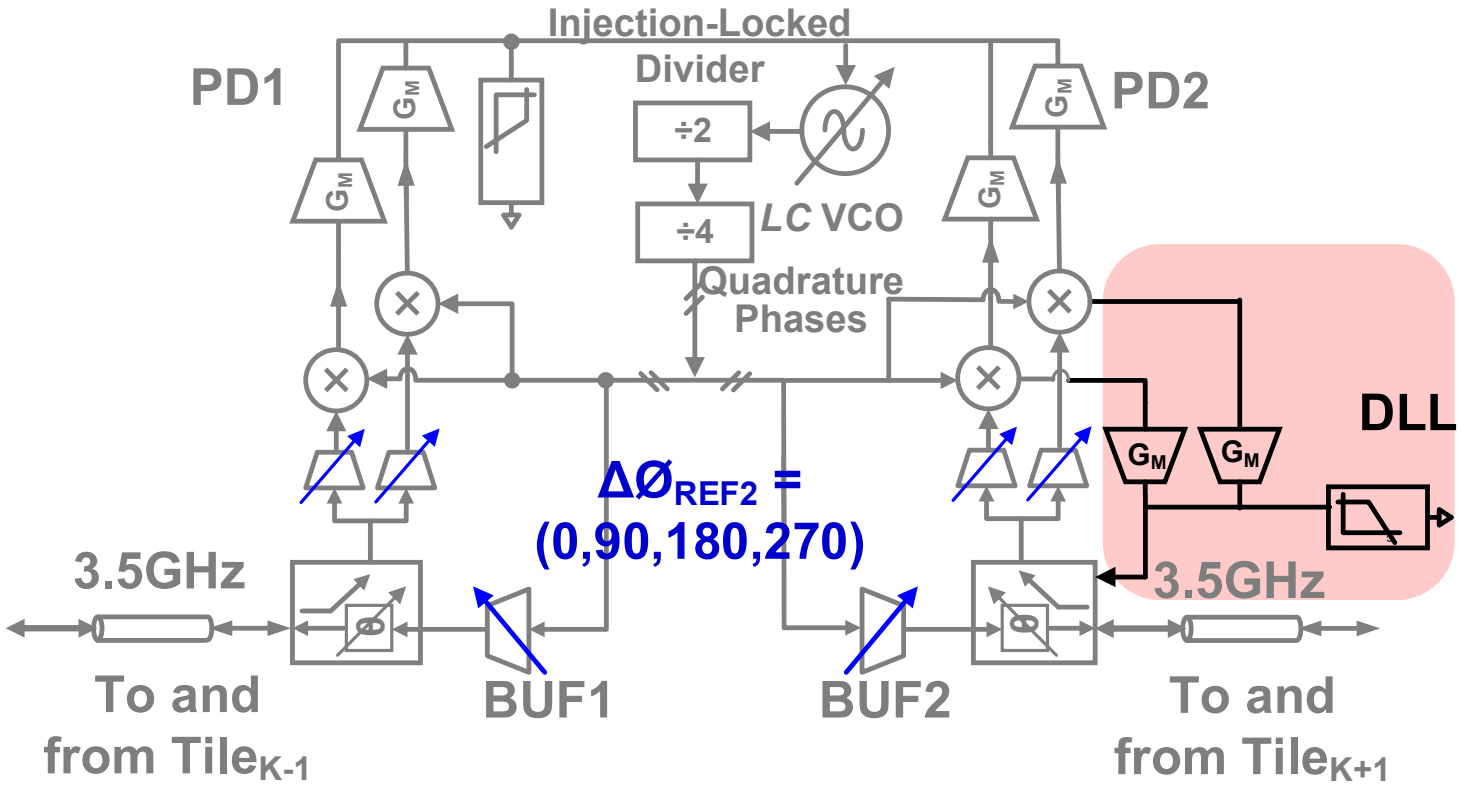


Dual-input 28GHz PLL: Phase Detector



- **Quadrature phase detector** further suppresses impact of output buffer signal leaking to PD input.

Dual-input 28GHz PLL: DLL Loop



- Since mixer-based PD is used, DLL ensures $\Delta\Phi_{PD2} = \pi/2$

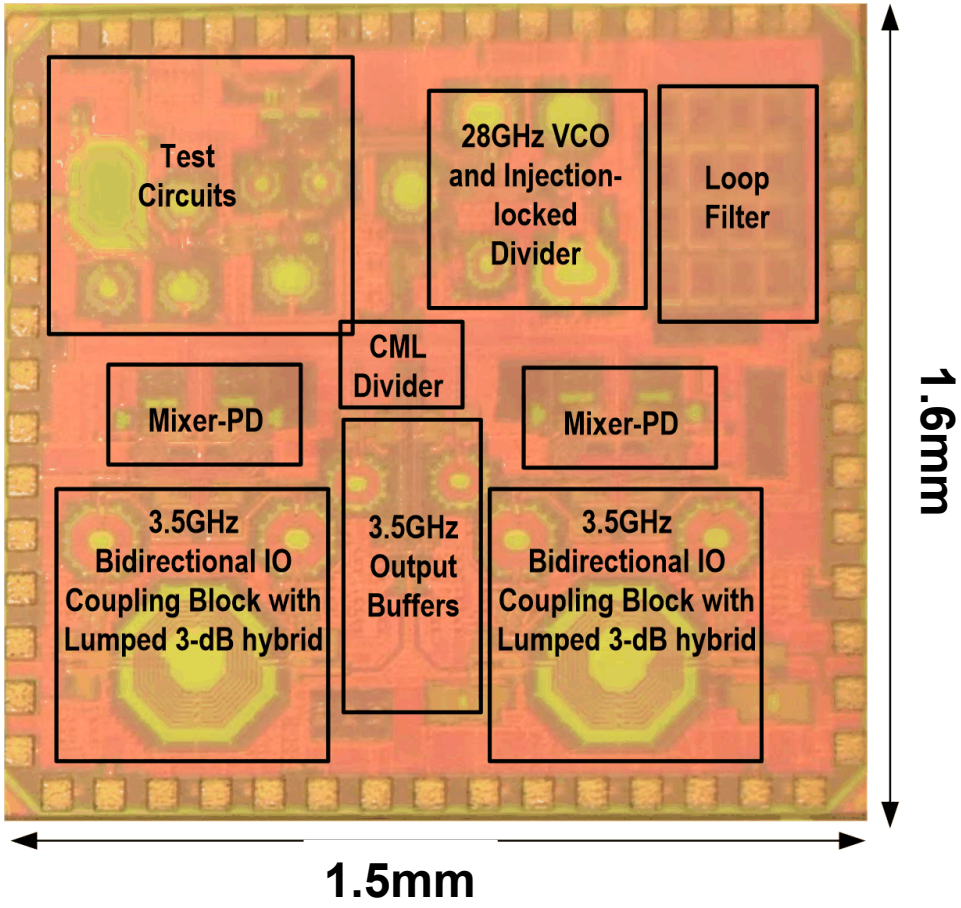
.

Outline

- Motivation
- Noise and Stability in Coupled-PLLs
- 28GHz Bidirectional Coupled-PLL in 65nm CMOS
- **Measured Performance**
- Conclusion and Future Work

Die Photo and Power Consumption

- Implemented in 65nm CMOS process with 3.4μm-thick top metal layer.
- Chip-on-board package (Rogers 4350B PCB).



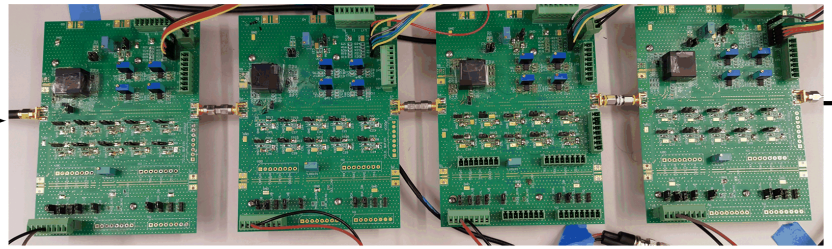
Block	Power Consumption [mW]
VCO	3.9
Buffer	7.9
ILFD	2.9
CML Buffer	29.3
IQ MXPD	10.5
DLL PD	0.1
PolyPhaseGm	24.6
Tx	7.7
Total	87

Test Setup

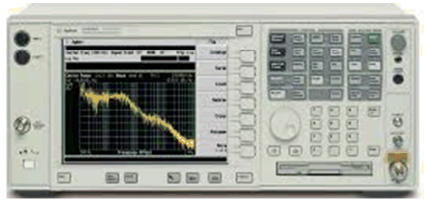
- Reference and measured clock are at 3.5GHz.

Anritsu MG3694C

Board 1 Board 2 Board 3 Board 4

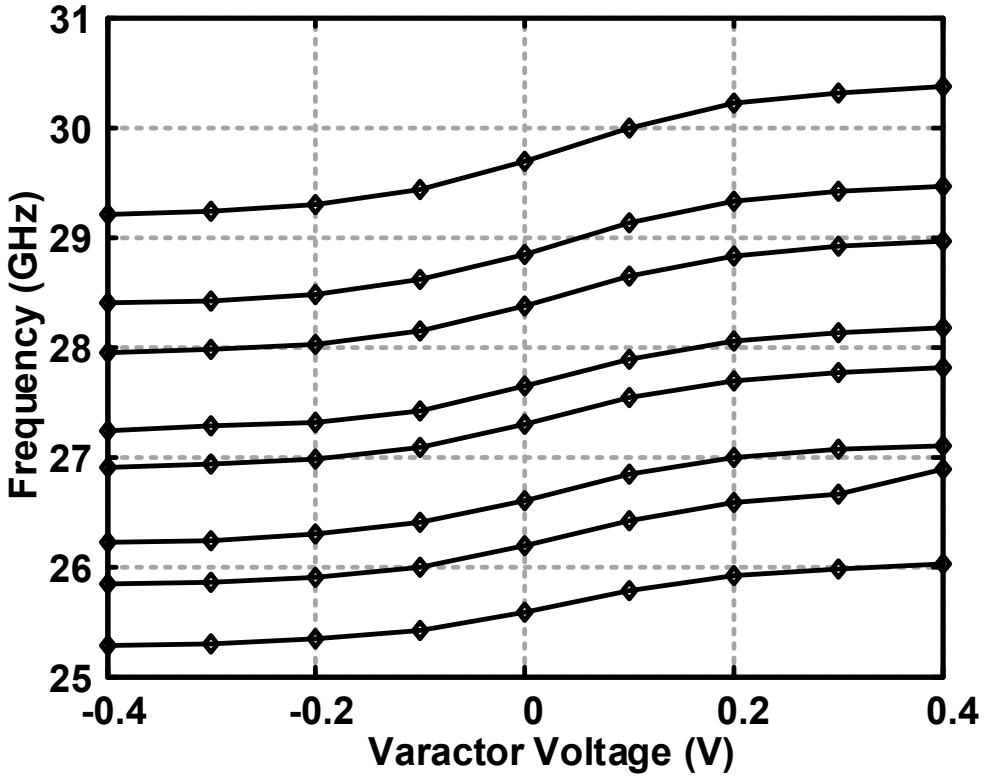


R&S FSUP26/ Agilent E4440A



Offset Frequency (MHz)	Reference Phase Noise (dBc/Hz)
0.1	-121
1	-127
10	-141

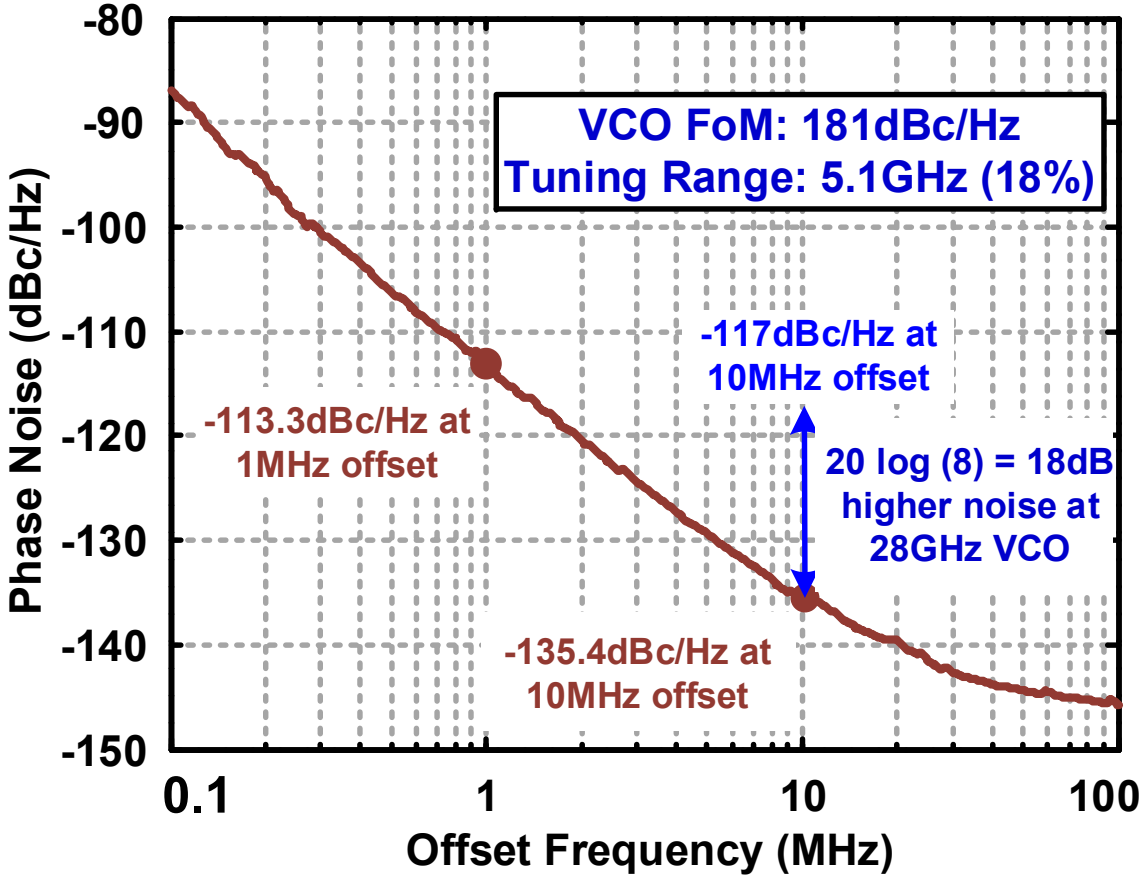
Measured VCO Tuning Range



Tuning Range: 25.3GHz to 30.4GHz (18% at 27.5GHz)
(8 coarse capacitance steps: ~ 0.9 GHz tuning in each step)

Measured VCO Phase Noise: Open-loop

Phase noise of VCO and divider chain output at 3.5GHz:



- VCO Phase noise: -135.4 dBc/Hz at 10MHz offset @3.5GHz
  → -117dBc/Hz at 10MHz offset @28GHz

PLL Phase Noise: Low-noise Reference

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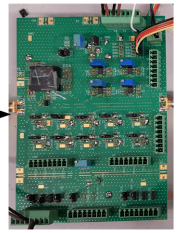
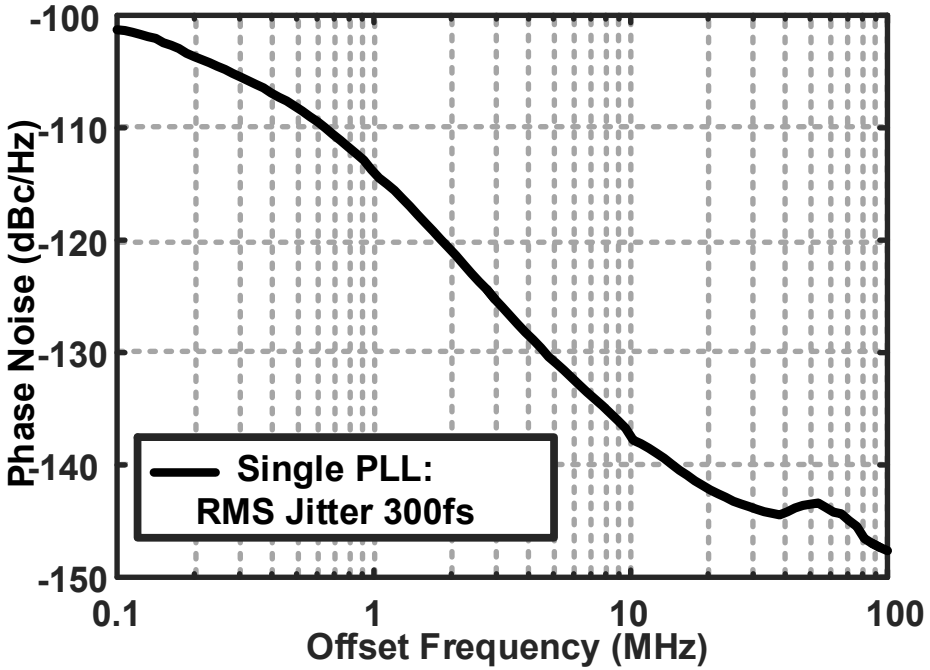
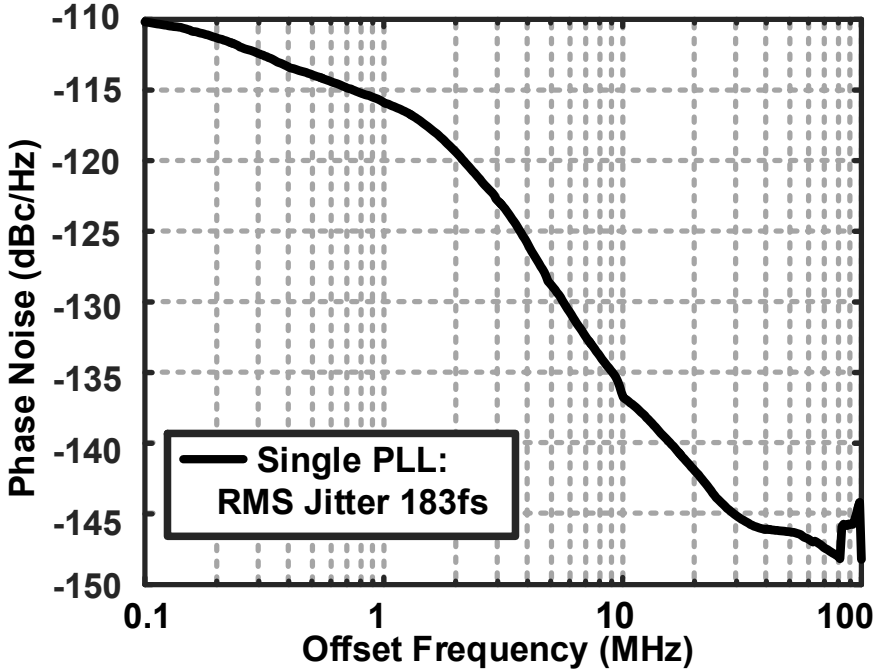


- Reference phase noise: -127 dBc@1 MHz offset.

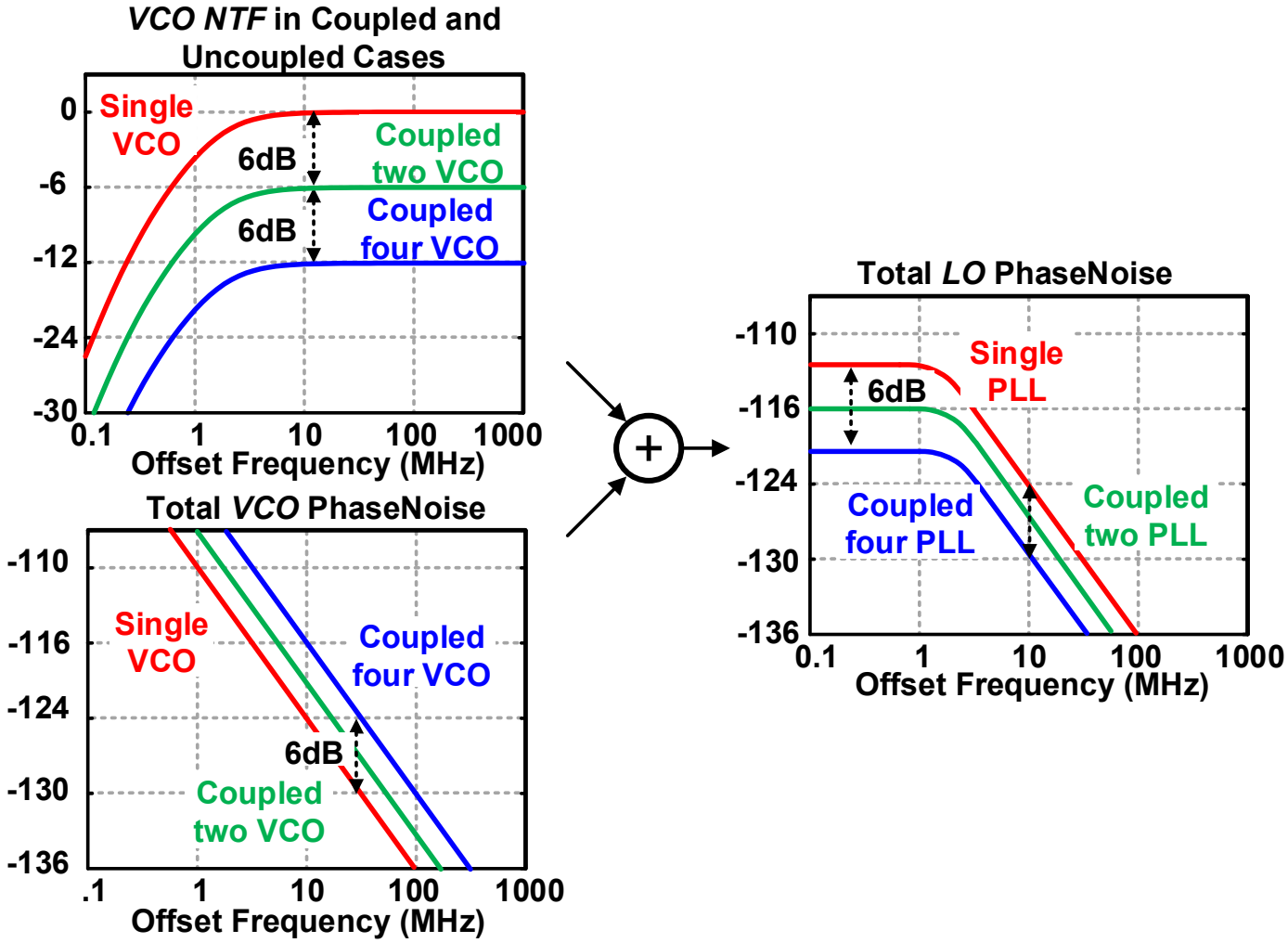
Loop Bandwidth: 1MHz



Loop Bandwidth: 3MHz



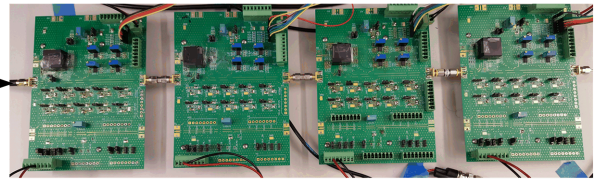
Phase Noise: Constant Ref Bandwidth



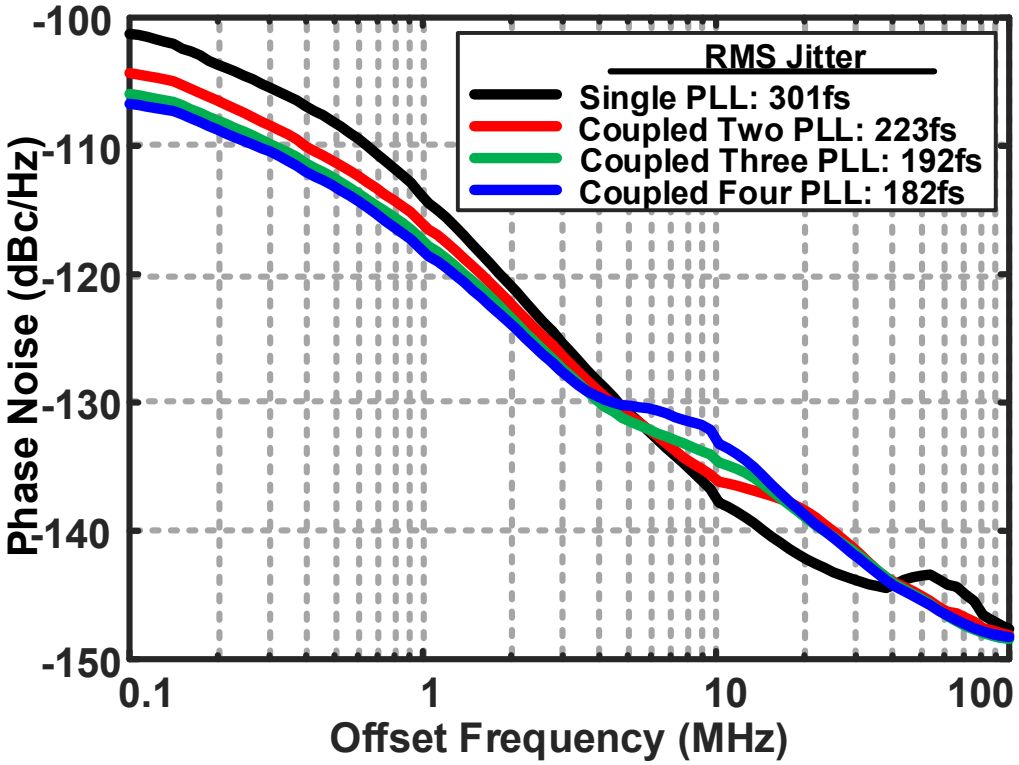
- If loop parameters ensure constant NTF pole; reference noise contribution is low → phase noise reduction with *N*

PLL Phase Noise: Low-noise Reference

Anritsu MG3694C



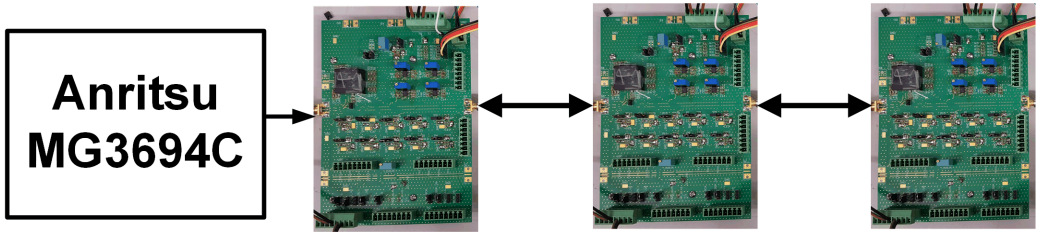
- Loop Bandwidth: 1MHz
- Reference phase noise: -127dBc/Hz @ 1MHz offset.



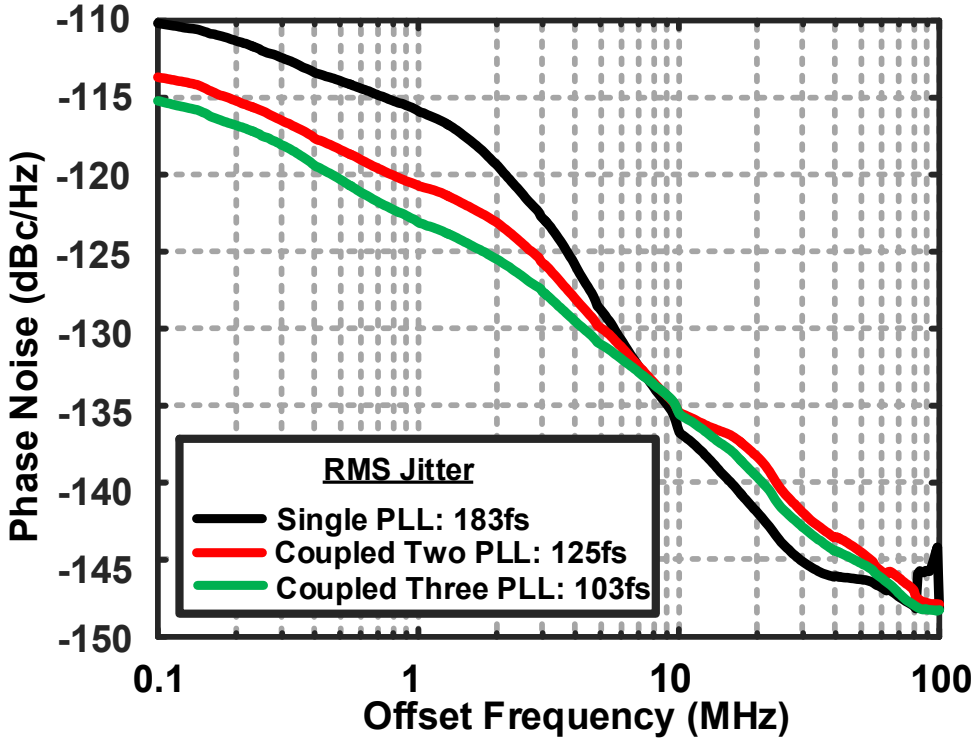
Phase noise Reduction $\propto 10logN$

Jitter integration bandwidth:
100KHz to 100MHz

PLL Phase Noise: Low-noise Reference



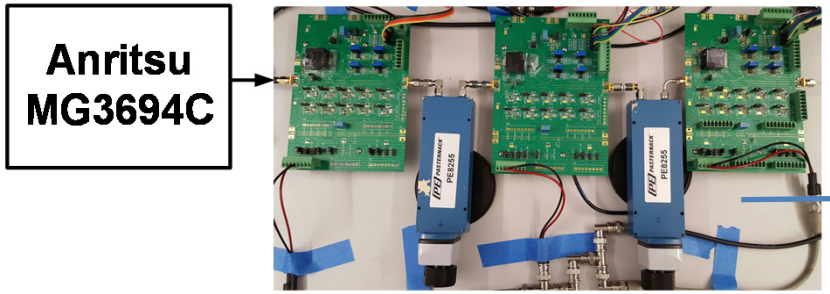
- Loop Bandwidth: 3MHz
- Reference phase noise: -127 dBc@1 MHz offset



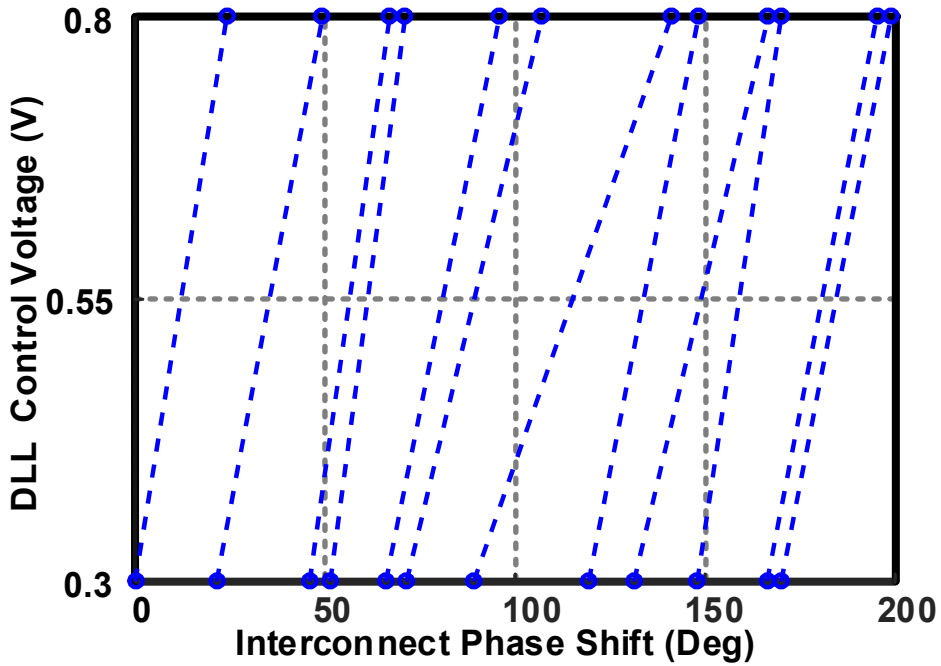
Phase noise Reduction $\propto 10logN$

Jitter integration bandwidth: 100KHz to 100MHz

Phase Offset in Interconnect

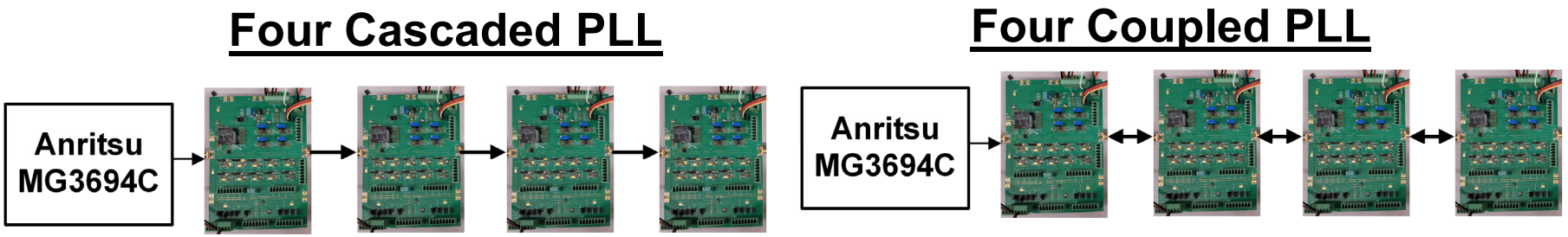


Variable phase shifter
(~210° range at 3.5GHz)

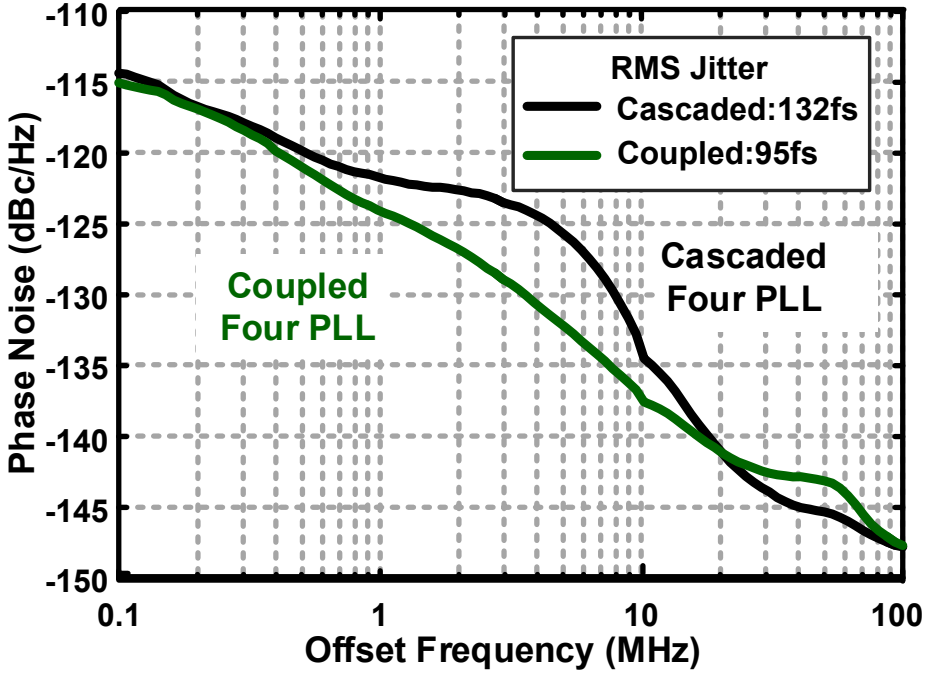


- DLL compensates for phase shift in the interconnect – control voltage changes in response to change in interconnect phase shift and coarse phase shift settings.

PLL Phase Noise: Low-noise Reference

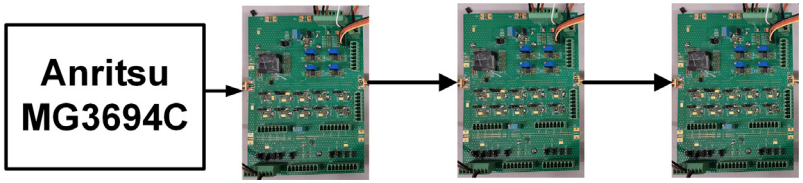


- Reference loop bandwidth selected such that in-band noise is constant.

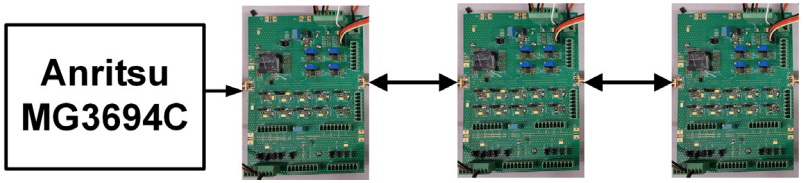


PLL Phase Noise: Low-noise Reference

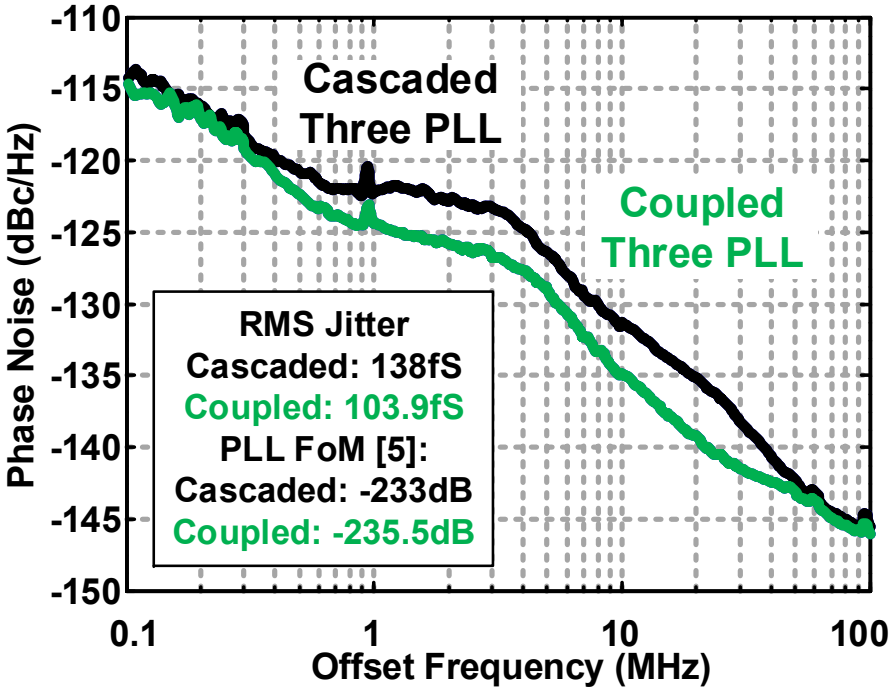
Three Cascaded PLL



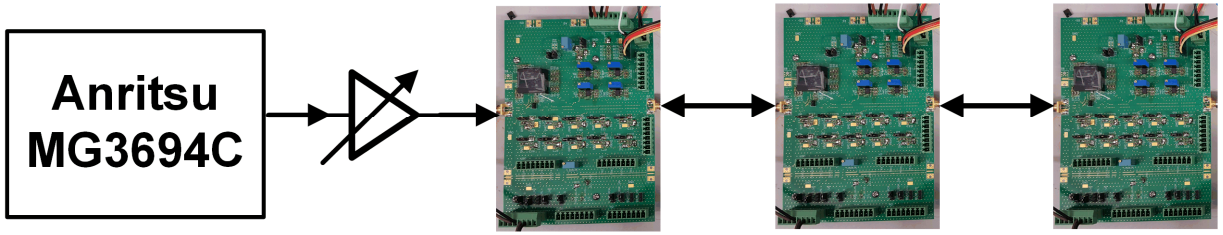
Three Coupled PLL



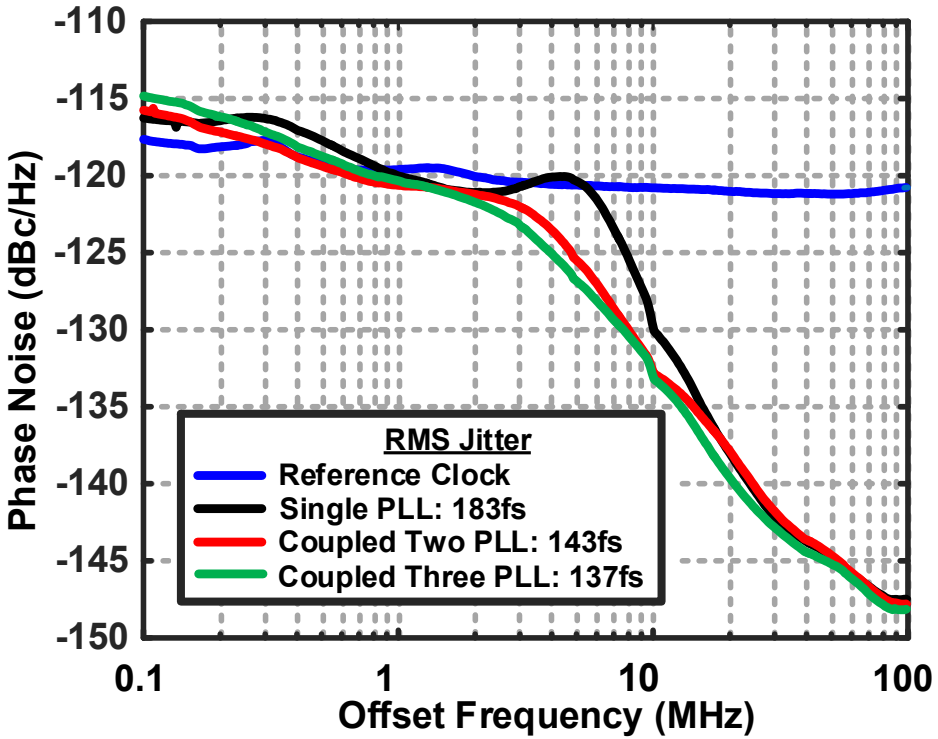
- Reference loop bandwidth selected such that in-band noise is constant.



Jitter Optimization: Noisy Reference



- Noisy reference provided to 3 boards coupled together to demonstrate jitter optimization.



Summary

- A scalable approach for bidirectional coupling presented for scalable mm-wave phased array/MIMO applications.
- Bidirectional coupling over a single-wire preserves simplicity of daisy-chain reference distribution while lowering phase noise.
- 28GHz prototype in CMOS demonstrates phase noise and jitter improvement with increasing number of PLLs.
- Future work includes incorporation of synchronization scheme in a scalable mm-wave array/MIMO transceiver.

Acknowledgements

- This work is supported by DARPA Arrays at Commercial Timescales (ACT) program.
- We acknowledge Rohde & Schwarz for measurement equipment support.

A 4.2us-Settling-Time 3rd-Order 2.1-GHz Phase-Noise-Rejection PLL Using A Cascaded Time-Amplified Clock-Skew Sub-Sampling DLL

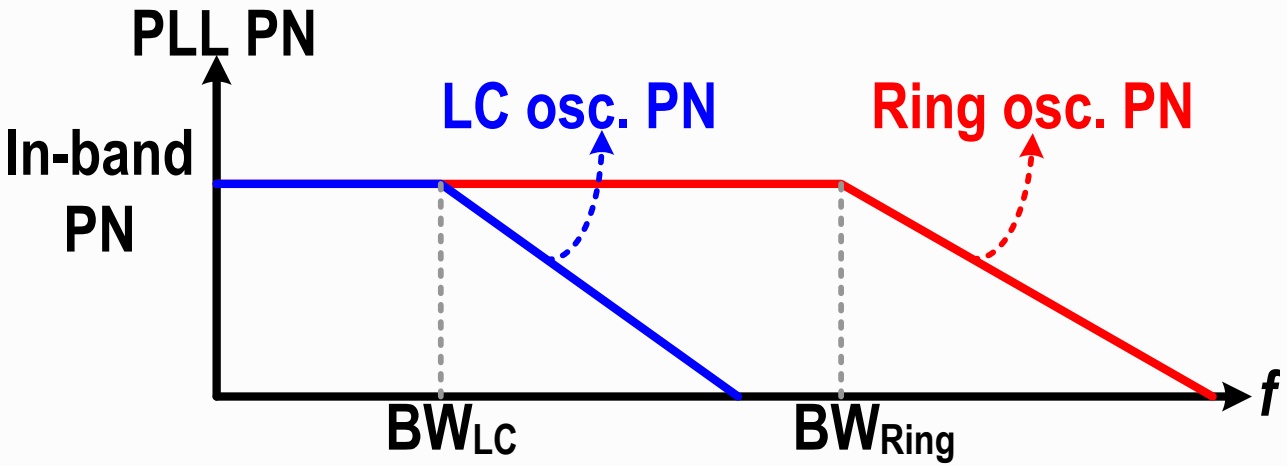
Zhiqiang Huang[1], Bingwei Jiang[1], Lianming Li[2], Howard C. Luong[1]

1. Hong Kong University of Science and Technology, Hong Kong
2. Southeast University, China

Outline

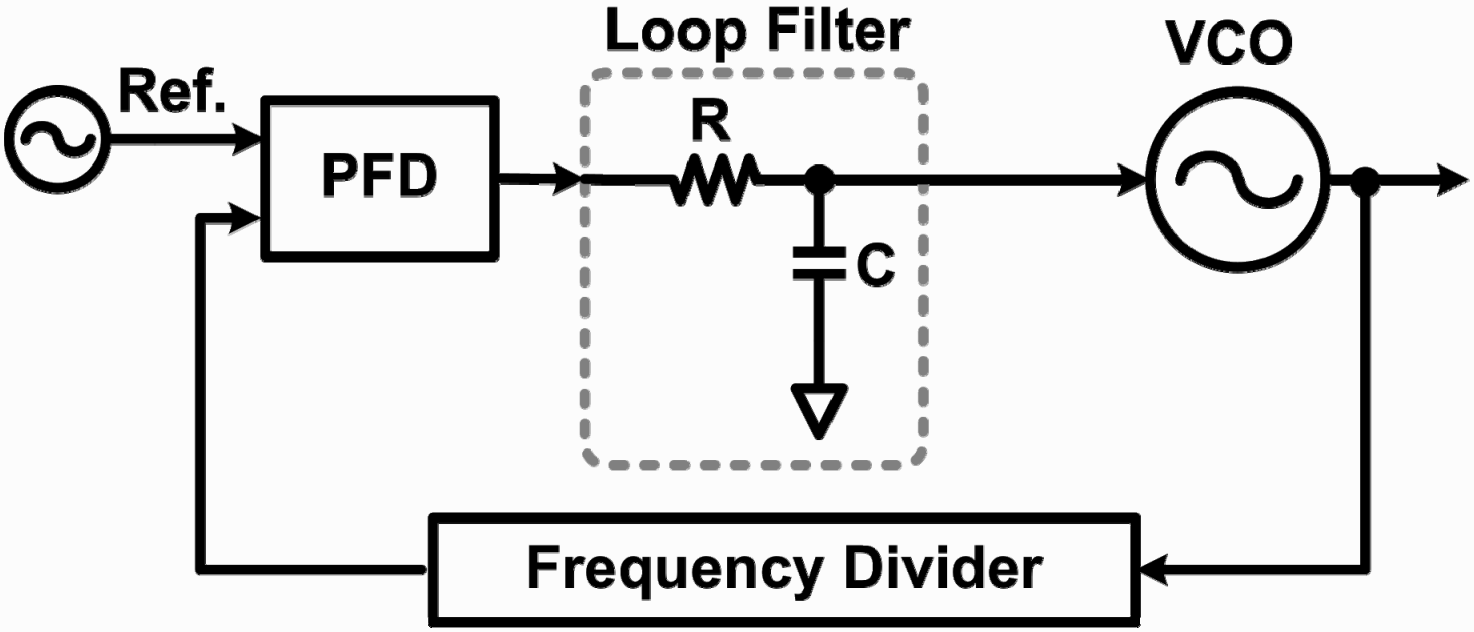
- ◊ Motivation
- ◊ Existing PLL Architectures
- ◊ Proposed Wide-Band High-Order Cascaded PLL
- ◊ Proposed Clock-Skew Sub-Sampling Phase Detector
- ◊ Measurement Results
- ◊ Conclusions

Motivation



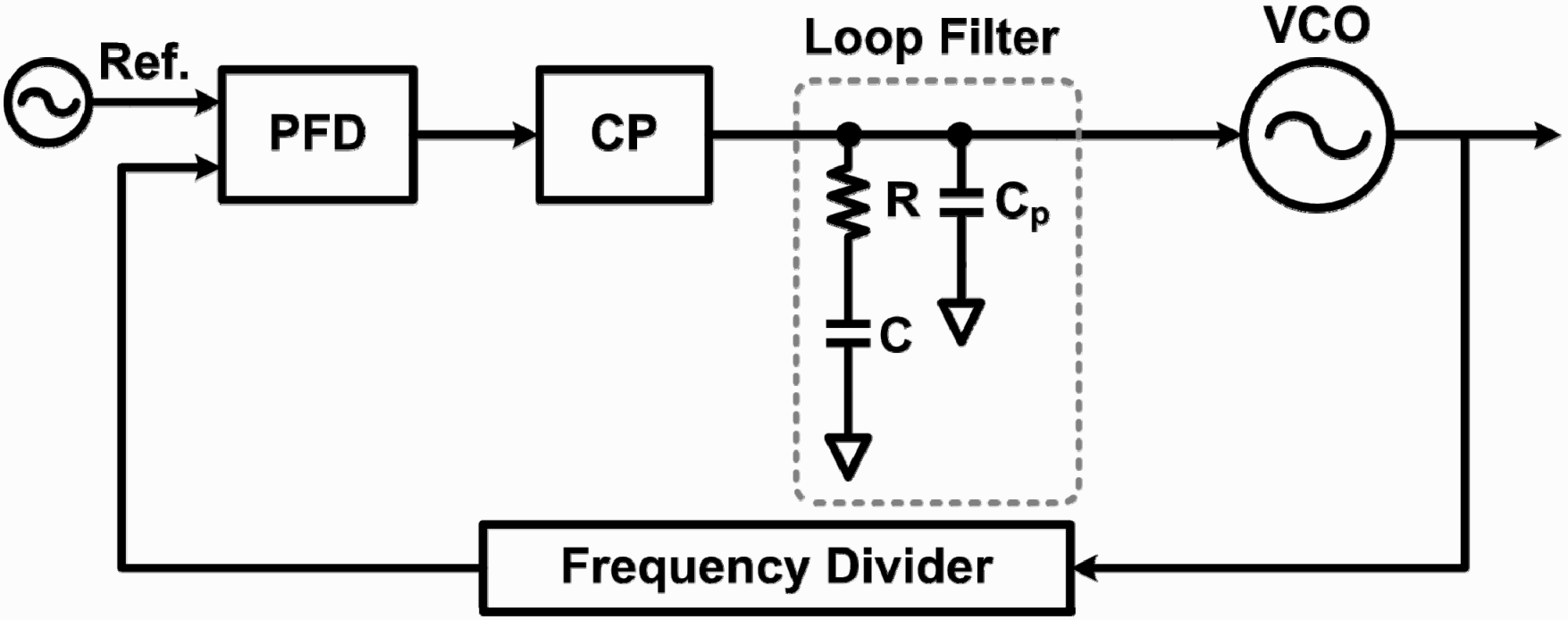
- ◊ Motivation: Low-noise compact PLL
- ◊ LC-oscillator-based PLLs
  - ✓ Good oscillator phase noise (PN)
  - × Inductor occupies large chip area
- ◊ Ring-oscillator-based PLLs
  - ✓ Compact chip area without large inductor
  - × Poor PN → Needs large loop bandwidth BW_{Ring} for minimum jitter
  - × Large frequency drift & sensitive to VCO's supply noise →Needs large loop gain

Existing PLL Architectures– Type-I PLL



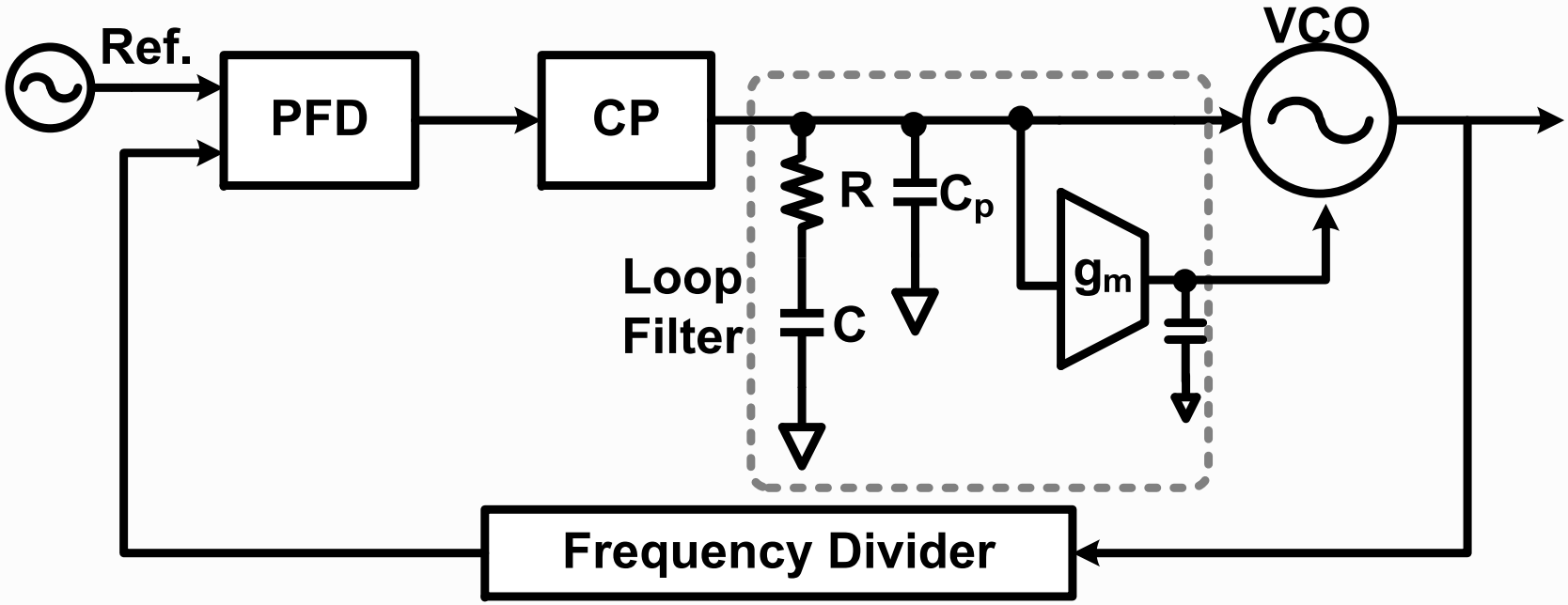
- ✓ 1st-order feedback loop has only 90^0 phase shift
  - → Large phase margin to support wide loop bandwidth to reject VCO's PN and cause fast settling time
- × Only one integrator in the feedback loop
  - →Low loop gain → Large frequency drift and sensitive to VCO supply noise

Existing PLL Architectures– Type-II PLL



- ✓ Two integrators in the feedback loop
  - →Larger loop gain →Smaller frequency drift and less sensitive to VCO supply noise
- × 2^{nd}-order feedback loop has phase shift close to 180^0
  - → smaller phase margin →narrower loop bandwidth for VCO's PN rejection and slower settling time

Existing PLL Architectures– Type-III PLL



✓ Three integrators in the feedback loop

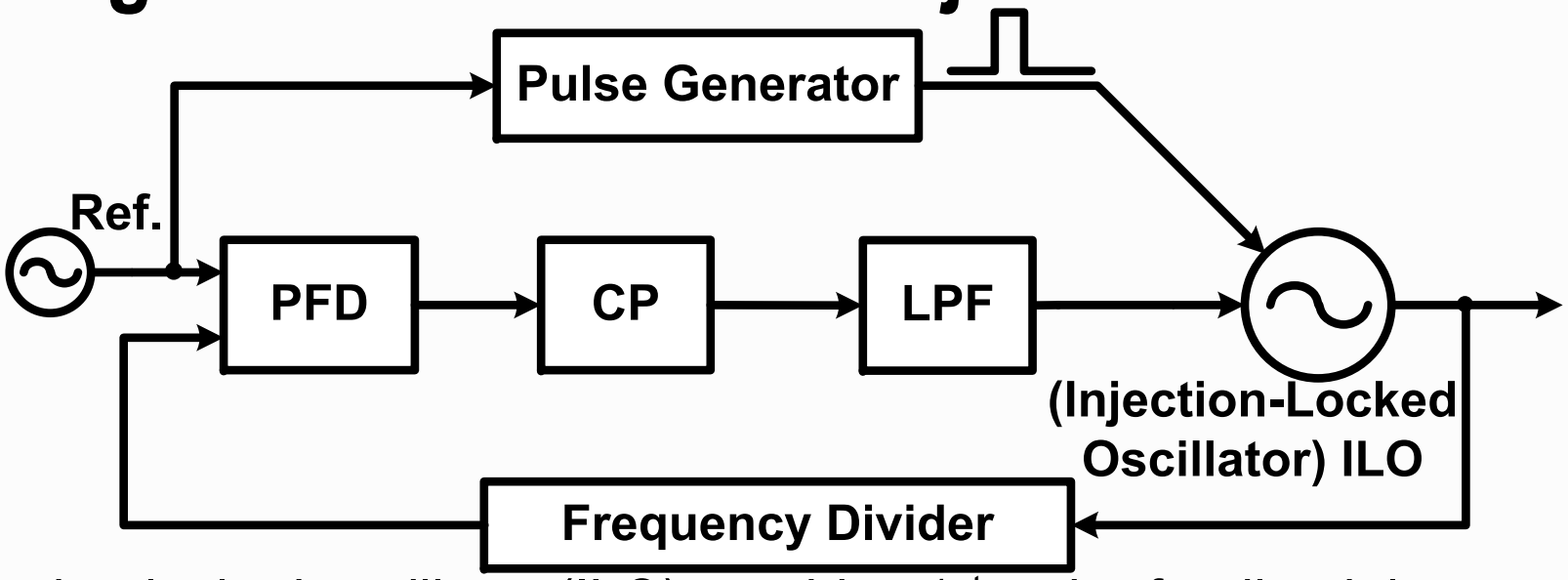
→Largest loop gain →Smallest frequency drift and minimum VCO's supply-noise sensitivity

× 3^{rd}-order feedback loop has phase shift >180^0

→ smallest phase margin →Narrow loop bandwidth & slow settling time

→Trade-off between loop bandwidth and loop order !

Existing PLL Architectures–Injection-Locked PLL

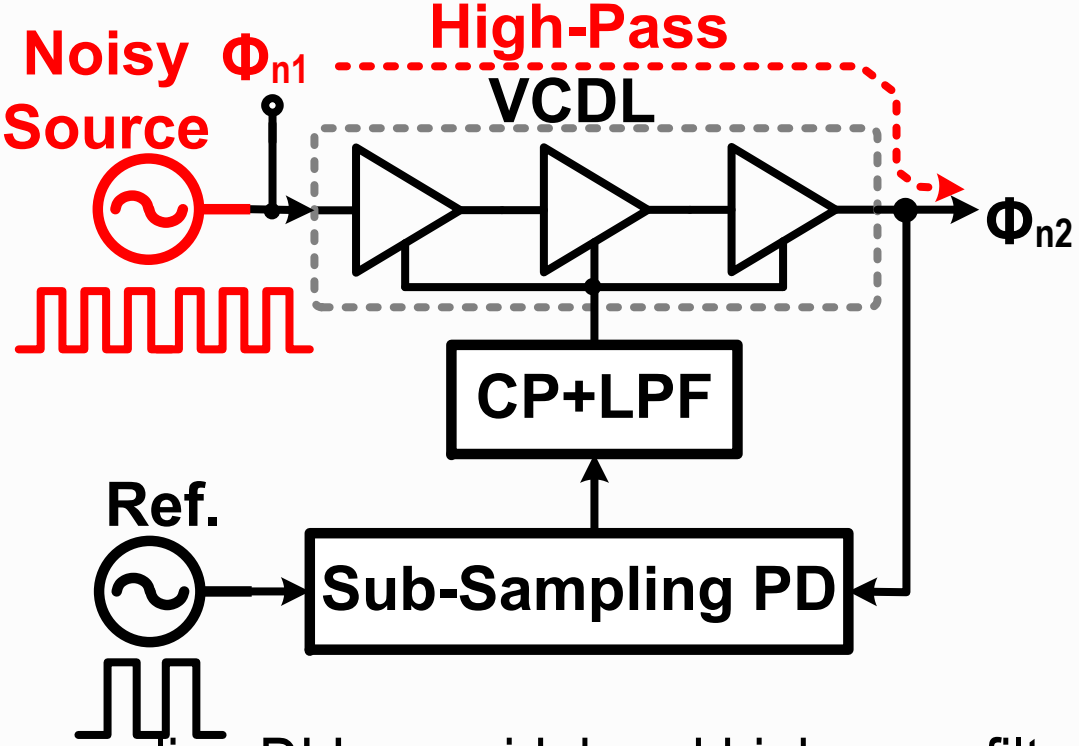


- ✓ Injection-locked oscillator (ILO) provides 1st-order feedback loop
  - →Wideband PN rejection for VCO
  - →Inserts 1st-order high-pass filter in PLL's feedback loop
- × Smaller PLL loop order
  - →Same order of PN rejection as regular PLL
- × Pulse generator directly injects into oscillator → Strong spurs
- × IL and PLL tends to lock oscillator at different output phase
  - → Reduce locking strength → Slow down settling time

Outline

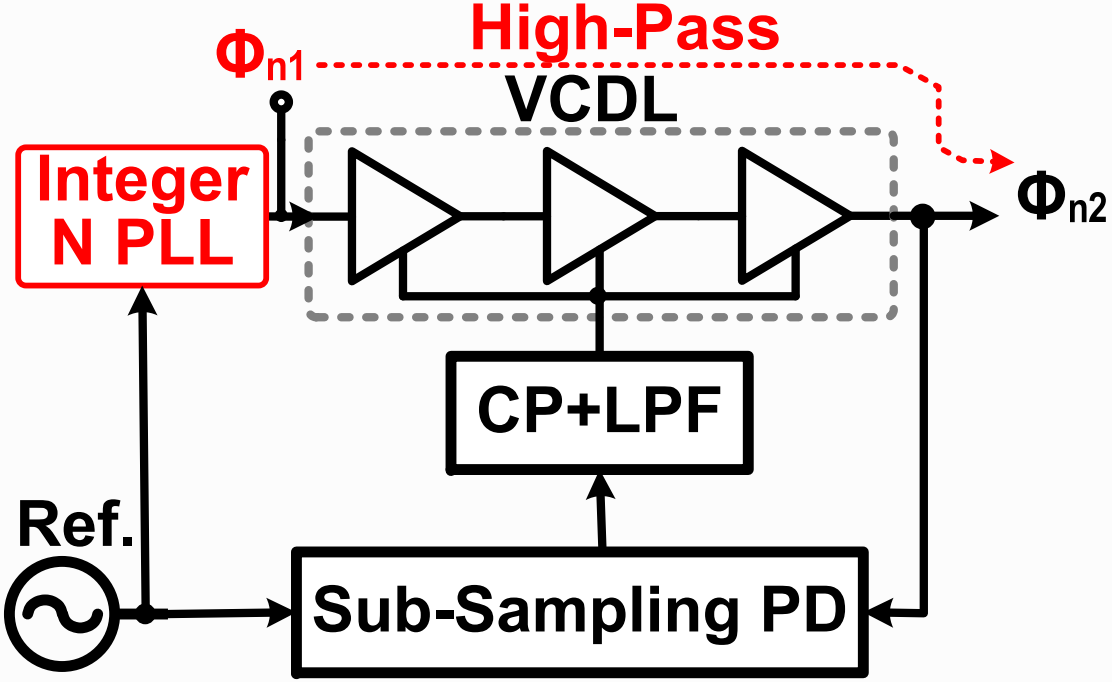
- ◊ Motivation
- ◊ Existing PLL Architectures
- ◊ **Proposed Wide-Band High-Order Cascaded PLL**
- ◊ Proposed Clock-Skew Sub-Sampling Phase Detector
- ◊ Measurement Results
- ◊ Conclusions

Sub-Sampling Delay-Locked Loop (DLL)



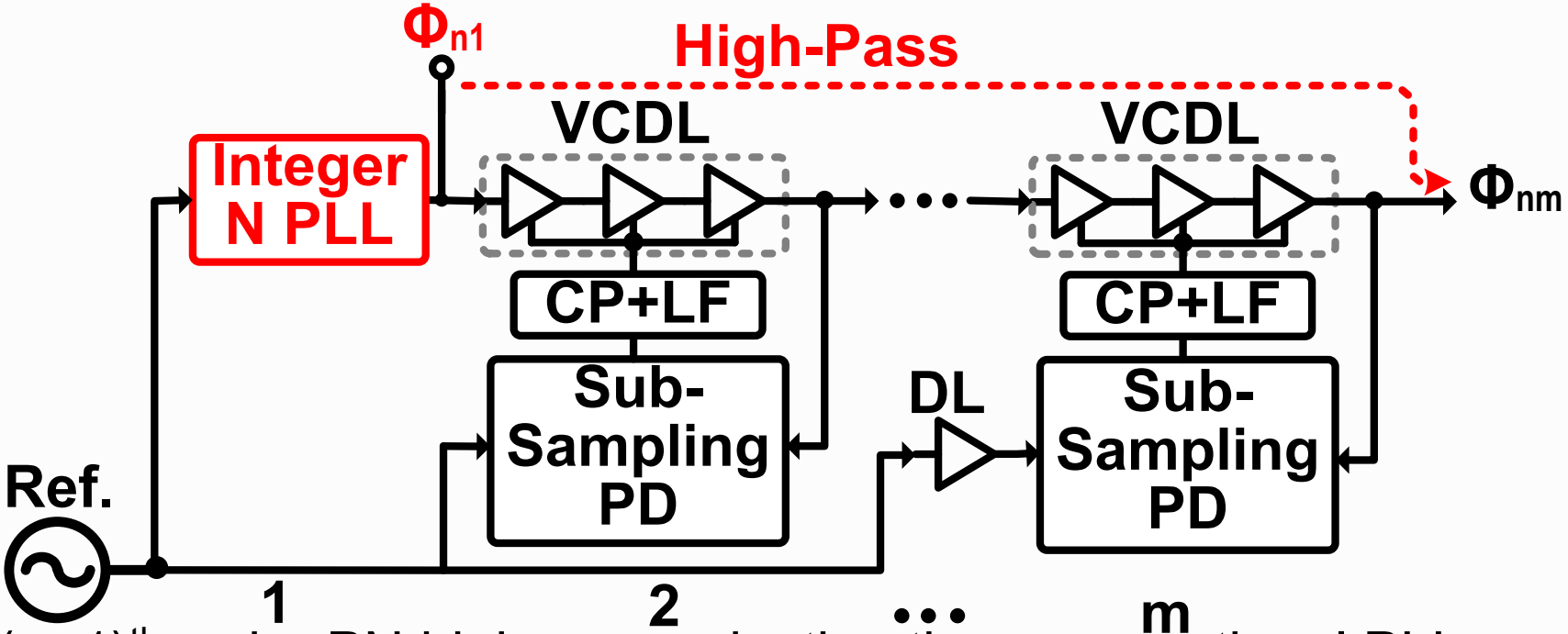
- 1st-order sub-sampling DLL → wideband high-pass filtering for Φ_{n1}
  - →Fast settling time
- Sub-sampling phase detector (PD)
  - →No frequency divider & good PN
- Voltage-controlled delay line (VCDL) covers input phase range

Cascaded PLL



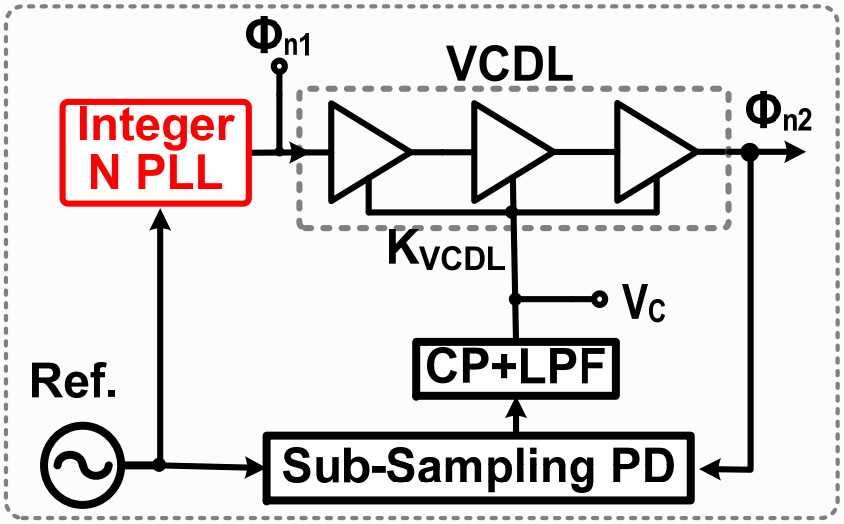
- One order higher PN high-pass rejection than conventional PLL
  → Higher loop gain → smaller noise, frequency drift and supply sensitivity
- 1st-order sub-sampling DLL
  →Wide loop bandwidth
- Total settling time depends on integer-N PLL and fast-settling sub-sampling DLL (sub-us)→ **small settling time degradation**

Multi-Stage Cascaded PLL



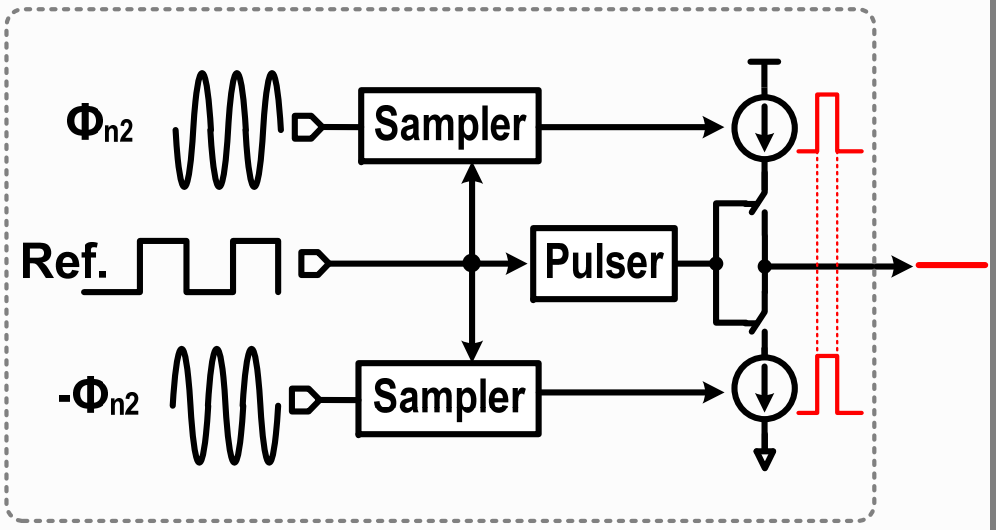
- ◊ $(m-1)^{th}$-order PN high-pass rejection than conventional PLL
  - → Extremely high loop gain
- ◊ All 1^{st}-order sub-sampling DLL s are connected by cascading
  - →No stability and bandwidth degradation → **Break trade-off!**
- ◊ Fast-settling sub-sampling DLLs
  - → **small settling time degradation**

Reference Spur



Cascaded PLL

$$\Phi_{n2} = \Phi_{n1} + K_{VCDL} V_C$$



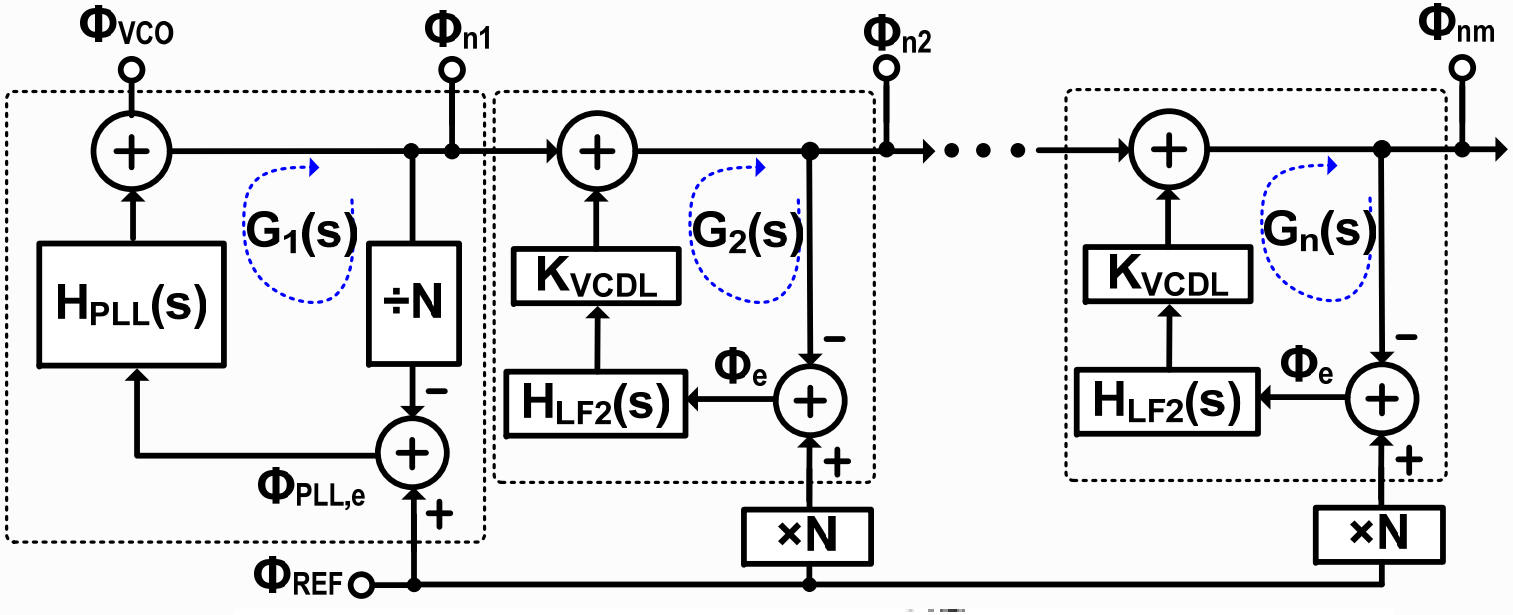
Sub-Sampling PD

[X. Gao, ISSCC'10]

- ◊ Reference spur depends on both integer-N PLL and sub-sampling DLL
- ◊ Sub-sampling PD
  - – CP current turned on/off simultaneously

  →No output charge in steady state → small reference spur degradation

Transfer Function



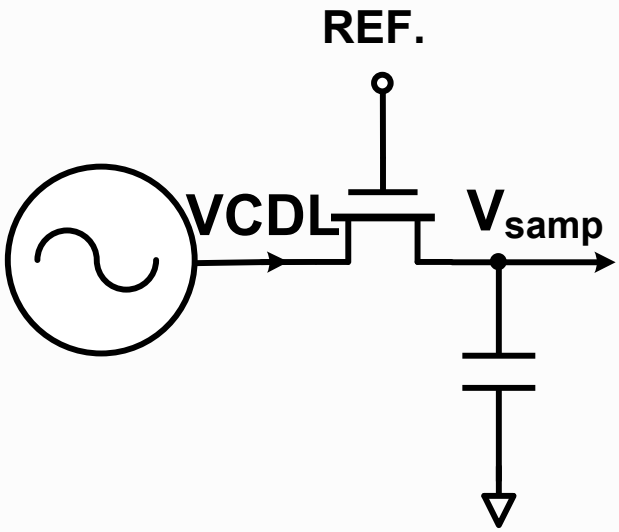
$$\Phi_{nm} \approx \frac{\Phi_{VCO}}{[1+G_1(s)][1+G_2(s)]\cdots[1+G_m(s)]} + \frac{N \cdot G_m(s) \cdot \Phi_{REF}}{1+G_m(s)} + \sum_{k=1}^{k=m-1} \frac{N \cdot G_k(s) \cdot \Phi_{REF}}{[1+G_k(s)][1+G_{k+1}(s)]\cdots[1+G_m(s)]}$$

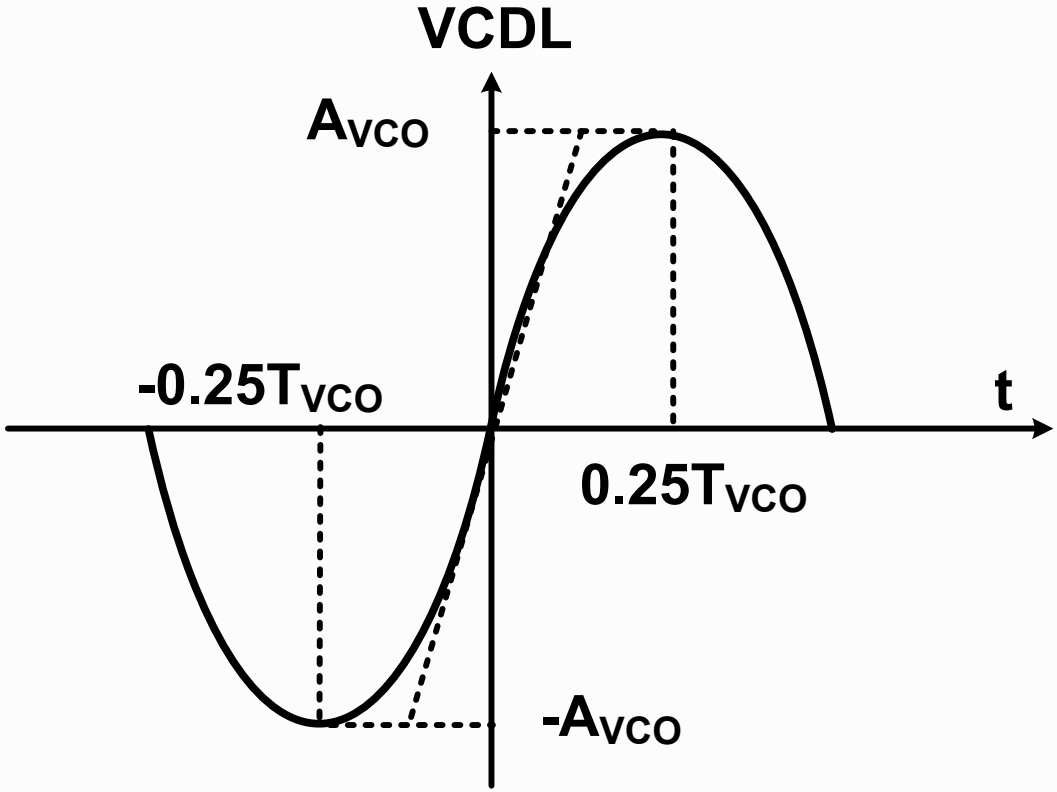
- ✓ High-order high-pass rejection for VCO's PN and frequency drift
- × 1st-order low-pass filtering for reference and charge-pump noise, even with more stages → limited suppression of out-band PN

Outline

- ◊ Motivation
- ◊ Existing PLL Architectures
- ◊ Proposed Wide-Band High-Order Cascaded PLL
- ◊ **Proposed Clock-Skew Sub-Sampling Phase Detector**
- ◊ Measurement Results
- ◊ Conclusions

Problems in Sub-Sampling Phase Detector (PD)



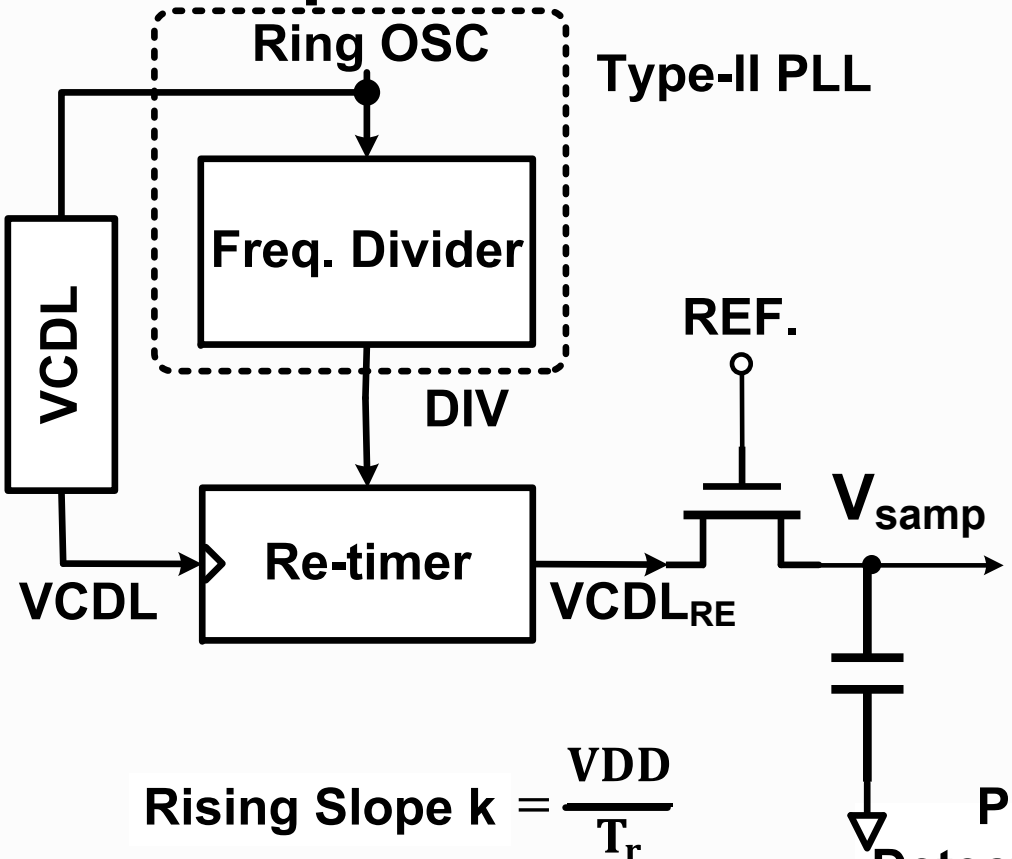


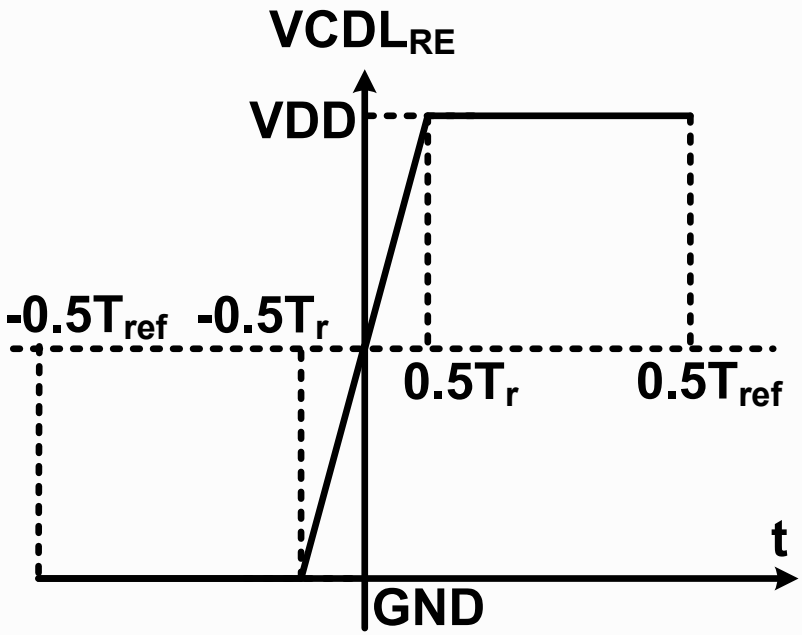
Rising Slope k $= \frac{2\pi A_{VCO}}{T_{VCO}}$

Phase Detection Gain $= \frac{T_{VCO}}{2\pi} k = A_{VCO}$

- ◊ Narrow detection range : +/- 0.25 T_{VCO}
- ◊ Gain limited by oscillation amplitude

Proposed Clock-Skew Sub-Sampling PD



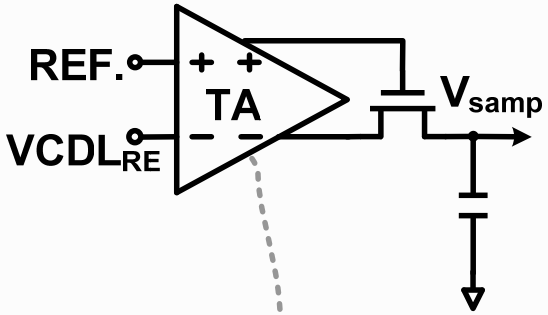


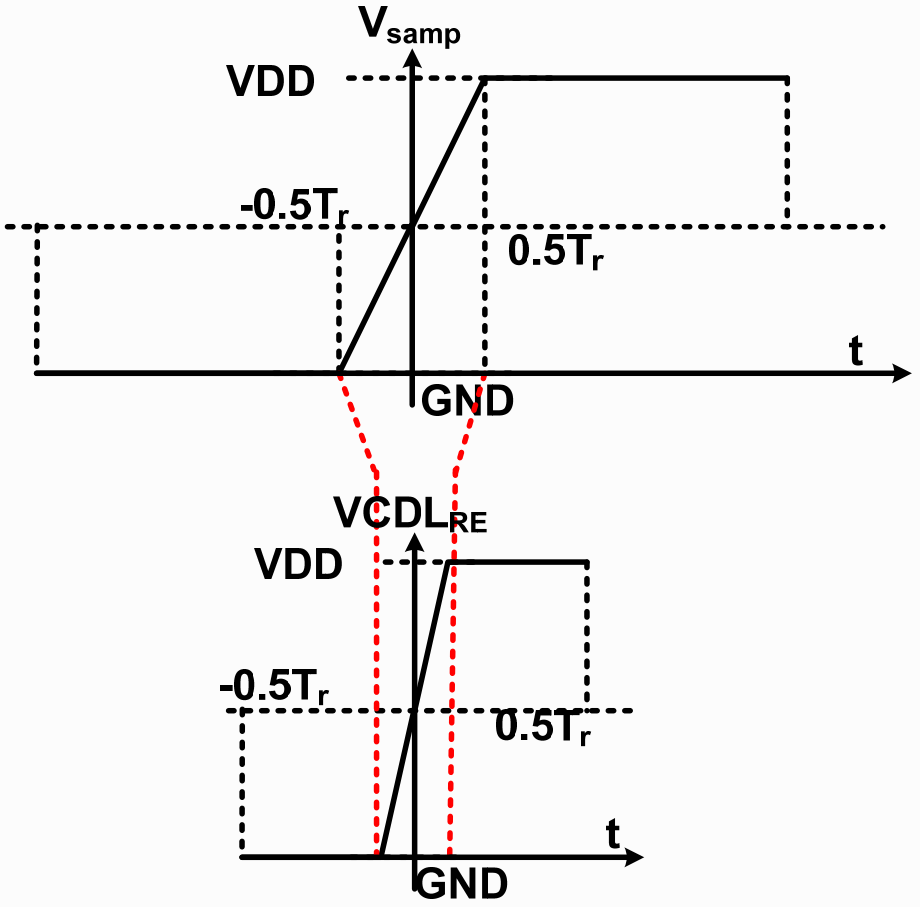
$$\text{Rising Slope } k = \frac{VDD}{T_r}$$

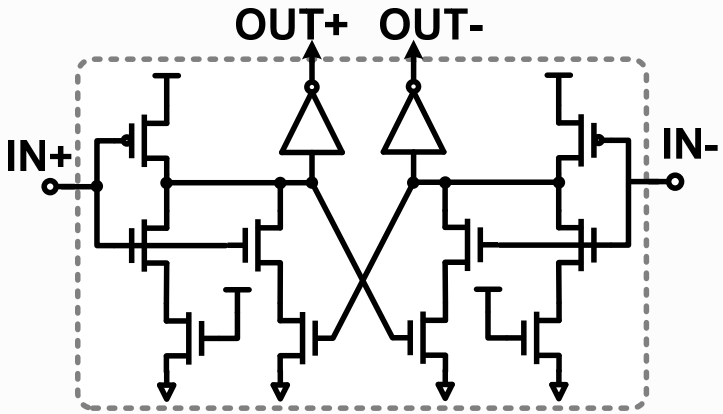
$$\text{Phase Detection Gain} = \frac{T_{VCO}}{2\pi} k = \frac{T_{VCO}}{2\pi} \cdot \frac{VDD}{T_r}$$

- ◊ Wide detection range : +/- 0.5 T_{ref}
- ◊ Gain can be boosted by reducing rising time of clock-skew, instead of increasing supply

Proposed PD with Time Amplifier







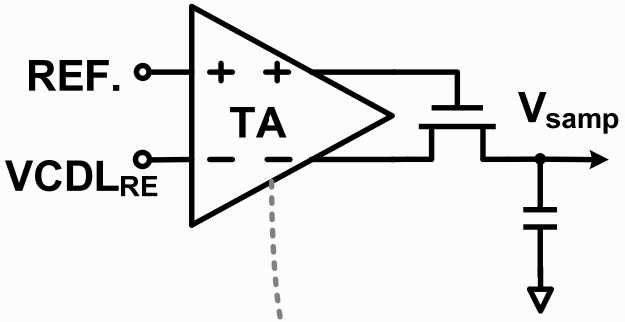
Time Amplifier (TA)

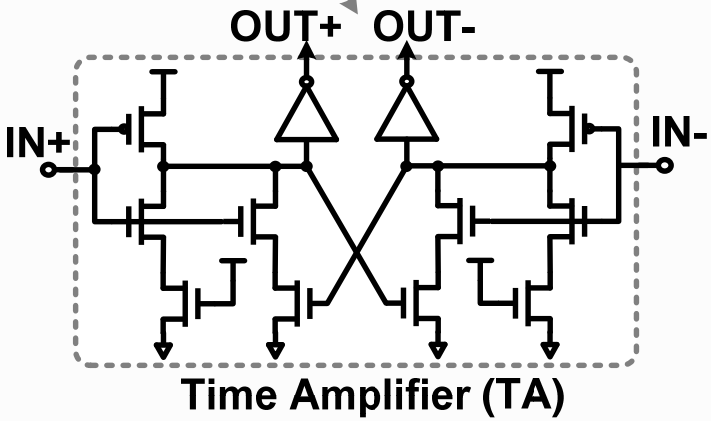
[S.-K. Lee, ISSCC'10]

◊ Wide dynamic range time-amplifier (TA) amplifies input time difference

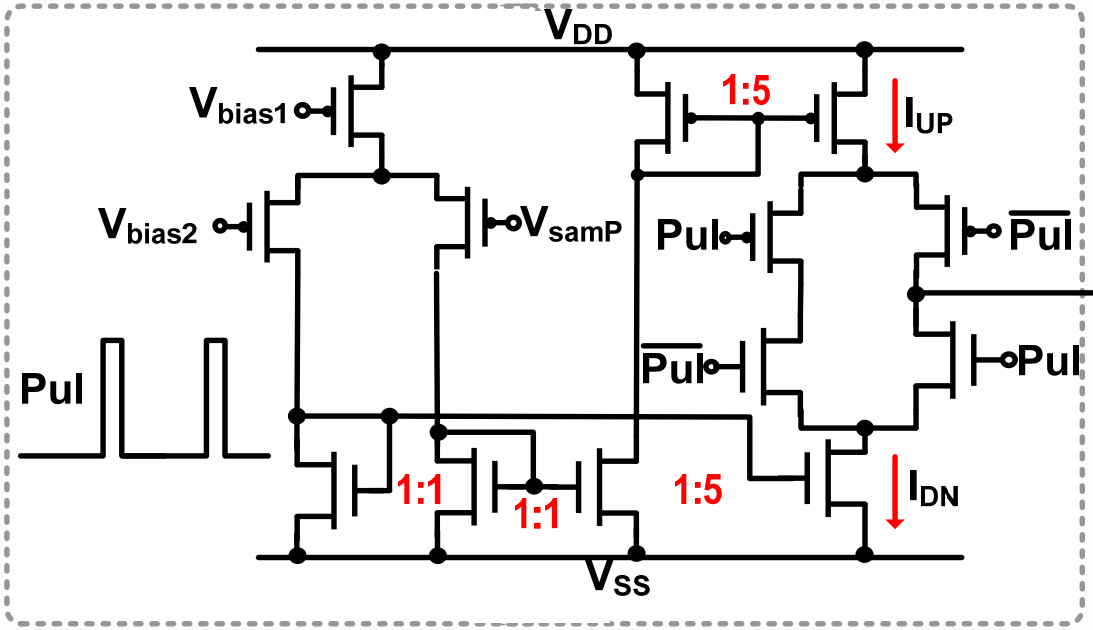
→Effectively reduces rising time → Boosts detection gain

Clock-Skew Sub-Sampling PD and Charge Pump





Time Amplifier (TA)



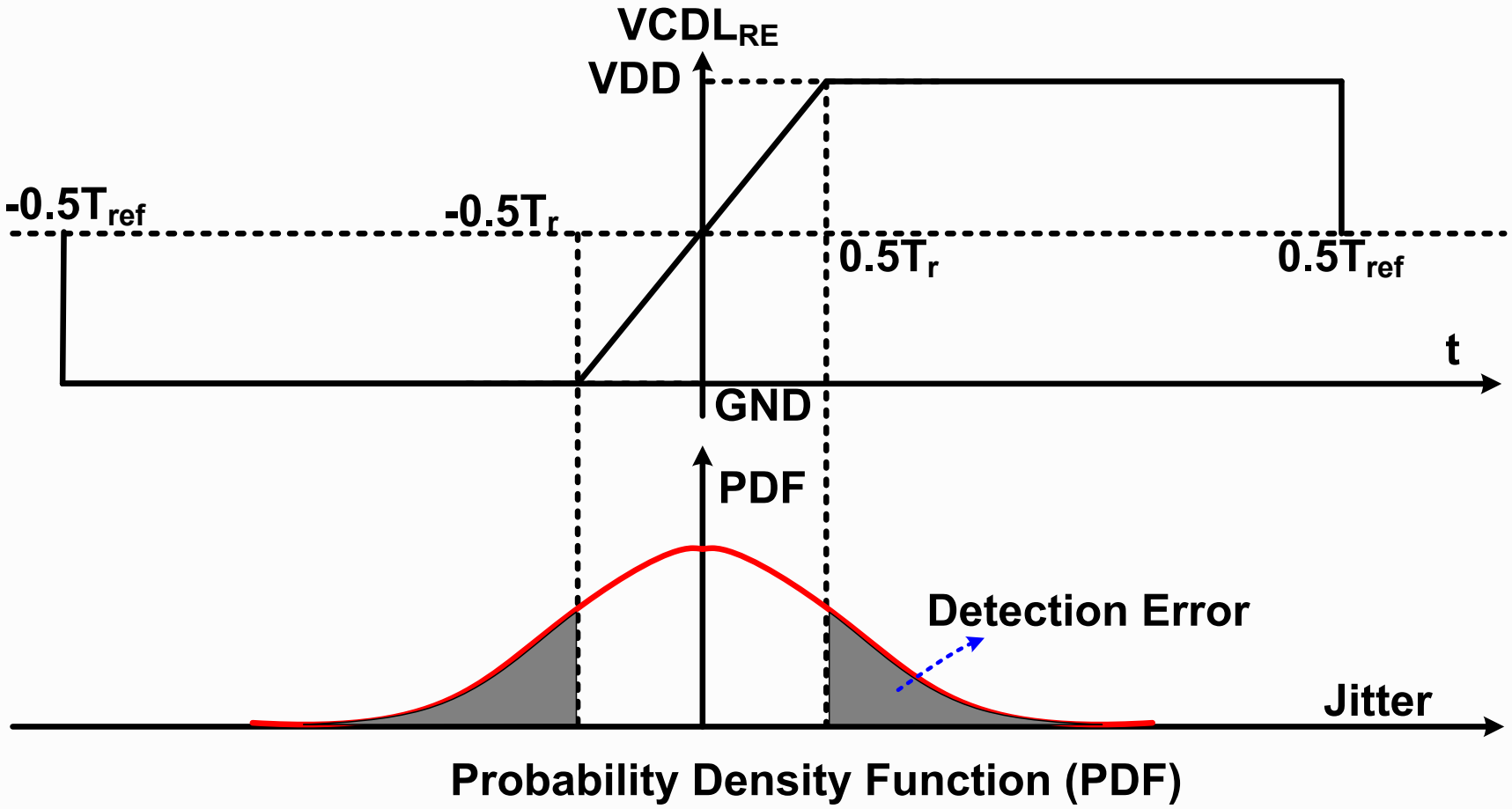
Charge Pump

[S.-K. Lee, ISSCC'10]

$$\text{Gain} = \frac{1}{2\pi f_{VCO}} \cdot \frac{TA \cdot VDD}{T_r} = \frac{5 \cdot 1.2V}{2\pi \cdot 2.1GHz \cdot 0.1ns} \approx 4V/rad$$

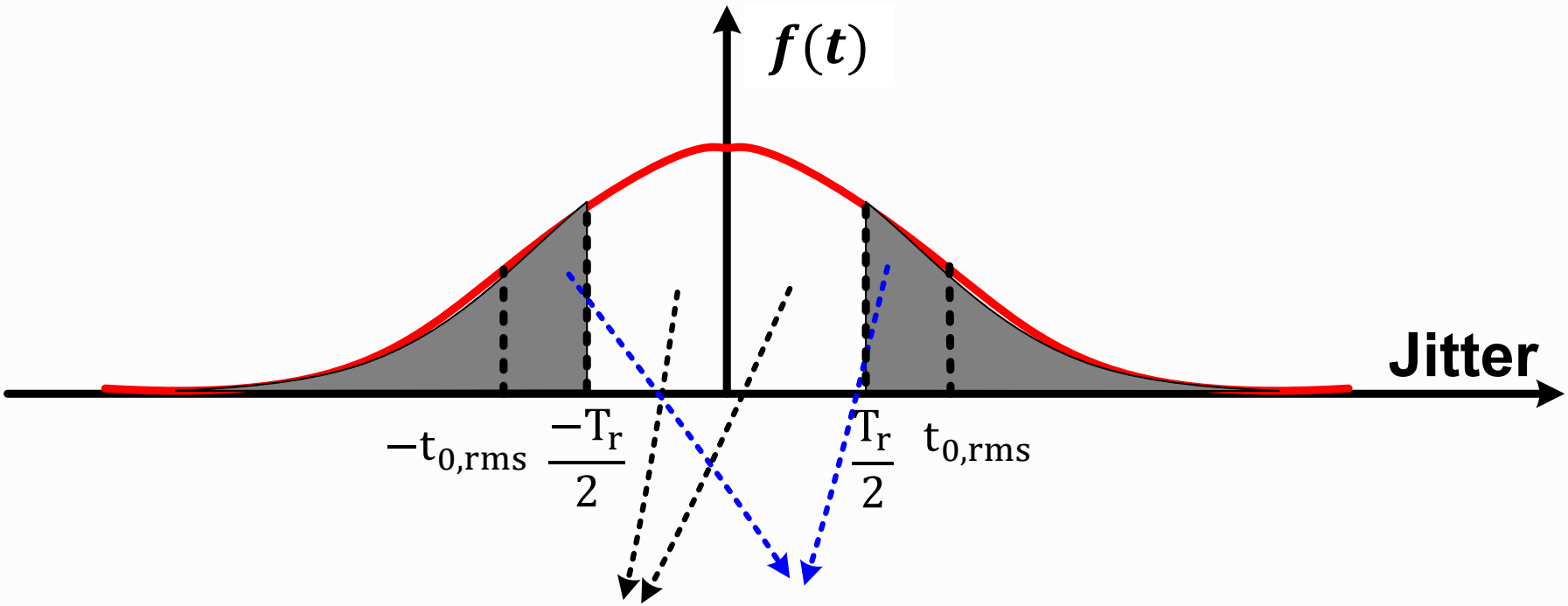
- 5 times TA gain, 100ps rising time of clock-skew, 1.2V supply
  - →Equivalent to sub-sampling PD with 4V amplitude 2.1GHz VCO
- I_{UP} and I_{DN} are turned on/off simultaneously → low ref. spur

Design Consideration – Linear Detection Region



- ◊ |Jitter|<0.5Tr, PLL behaves as linear PLL
- ◊ |Jitter|>0.5Tr, clock-skew sub-sampling PD behaves as bang-bang PD → introduces quantization noise

Average Gain of Clock-Skew Sub-Sampling PD

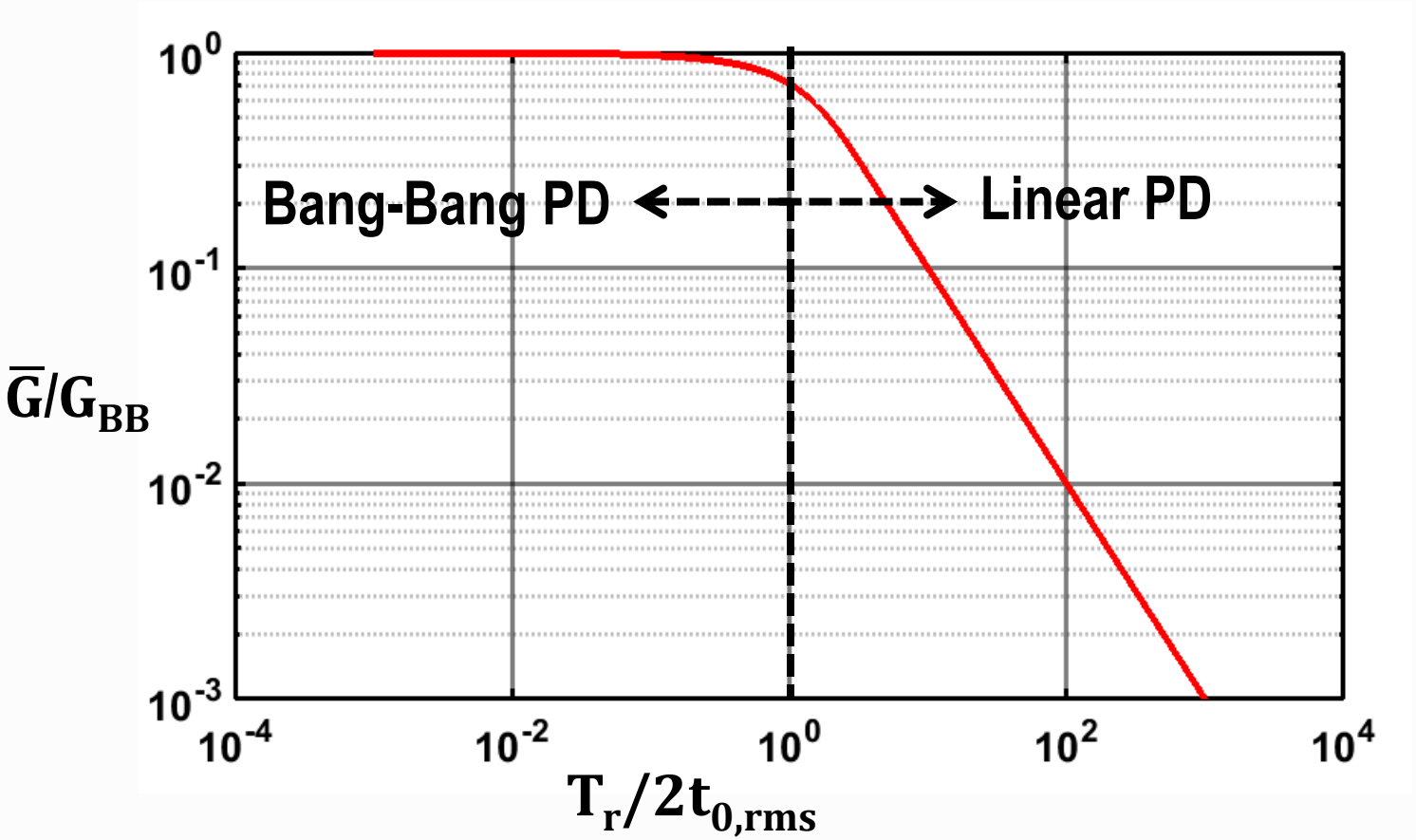


- Linear jitter t_1
- Linear gain: $G_1 = \frac{V_{DD}}{T_r}$

- Nonlinear jitter t_2
- Bang-Bang PD gain: $G_{BB} = \frac{V_{DD}}{2t_{0,rms}}$

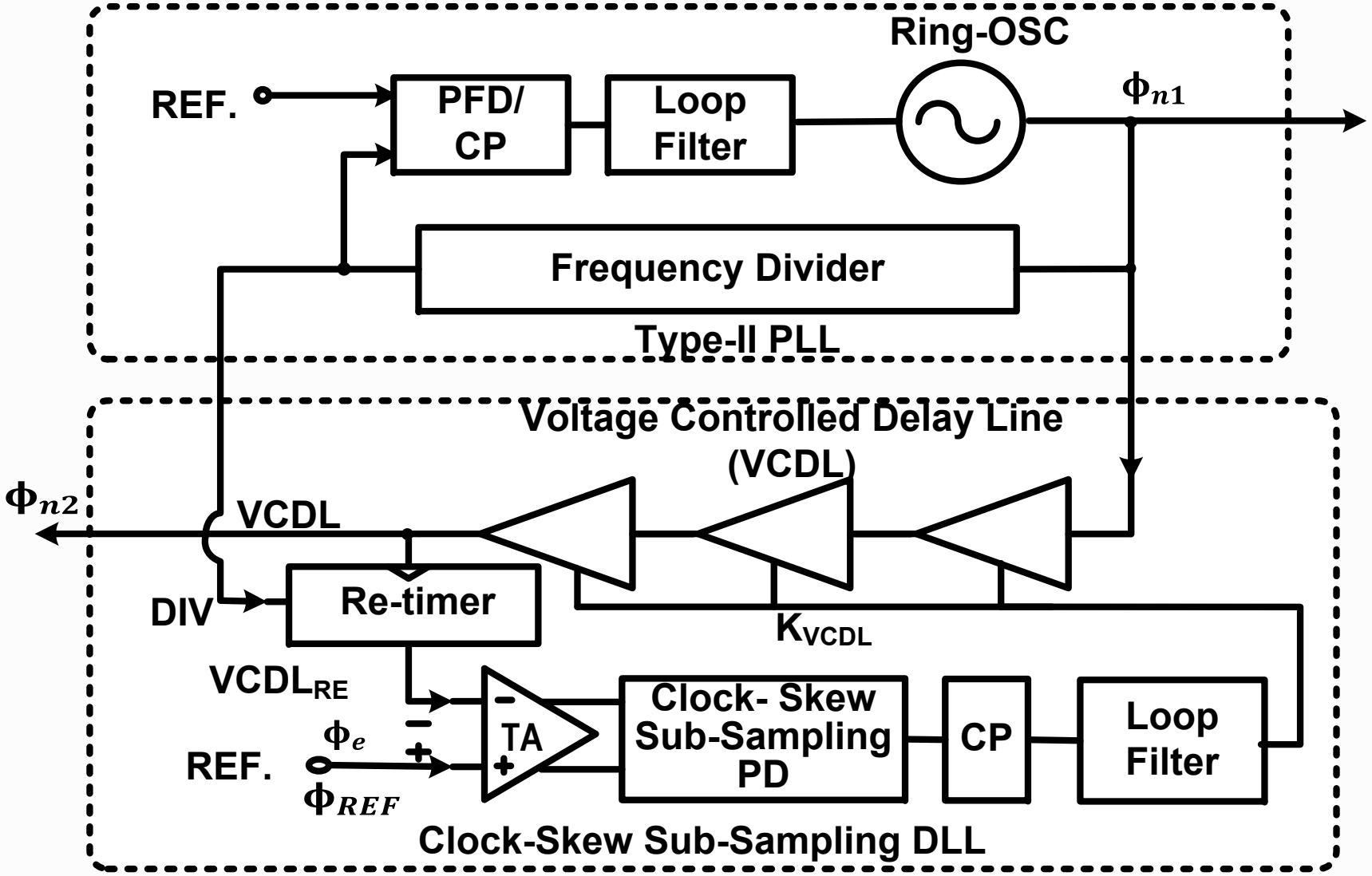
$$\overline{G} = \frac{\sqrt{2\int_0^{0.5T_r} t_1^2 G_1^2 f(t_1)dt_1 + 2\int_{0.5T_r}^{\infty} 0.25V_{DD}^2 f(t_2)dt_2}}{t_{0,rms}}$$

Average Gain Calculation

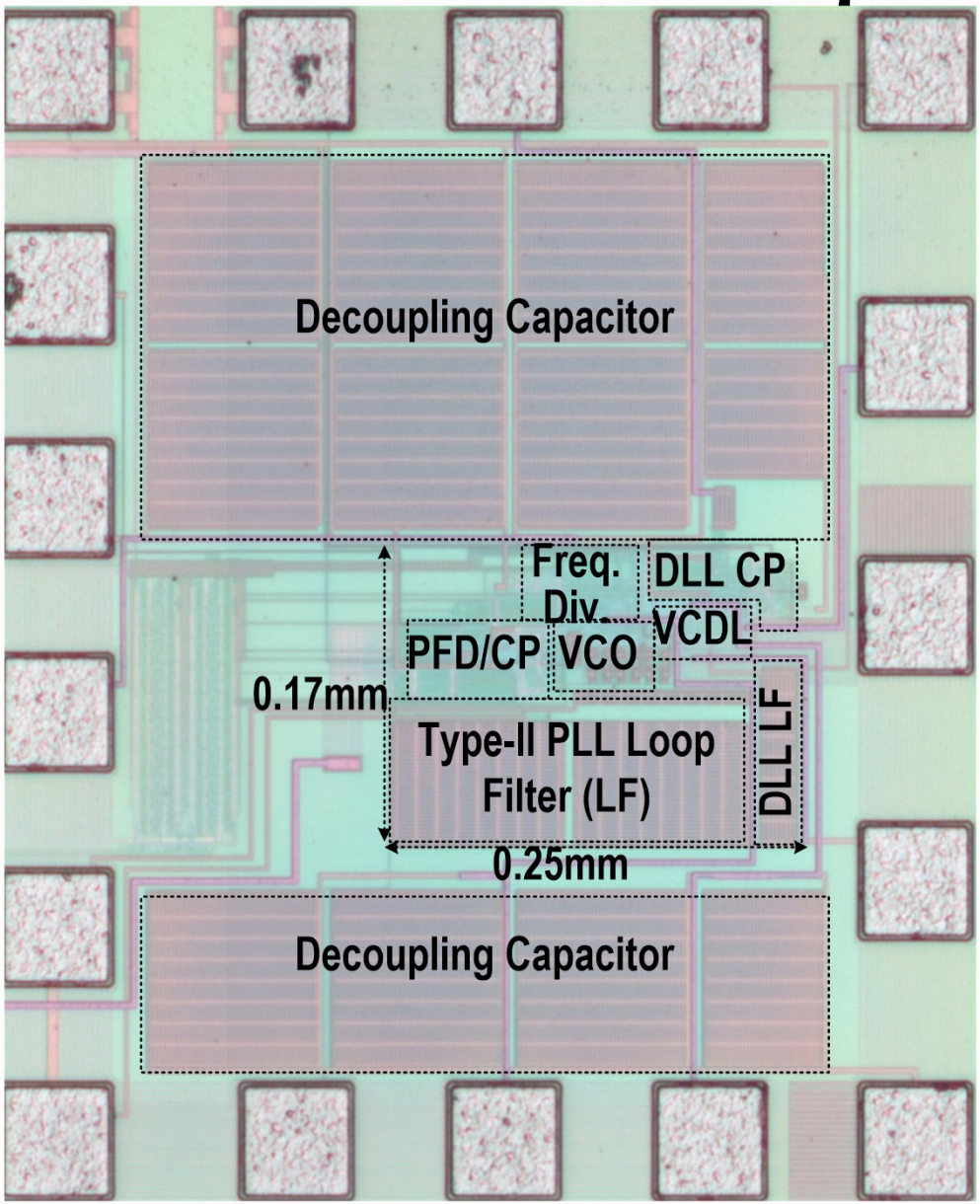


- ◊ Smaller rising time $T_r \rightarrow$ larger average gain
- ◊ $T_r < 2t_{0,rms} \rightarrow$ average gain is maximum: G_{BB}
- ◊ T_r approaches 0 $\rightarrow$ bang-bang PD & larger detection error

Block Diagram of 2-Stage Cascaded PLL



Chip Photo

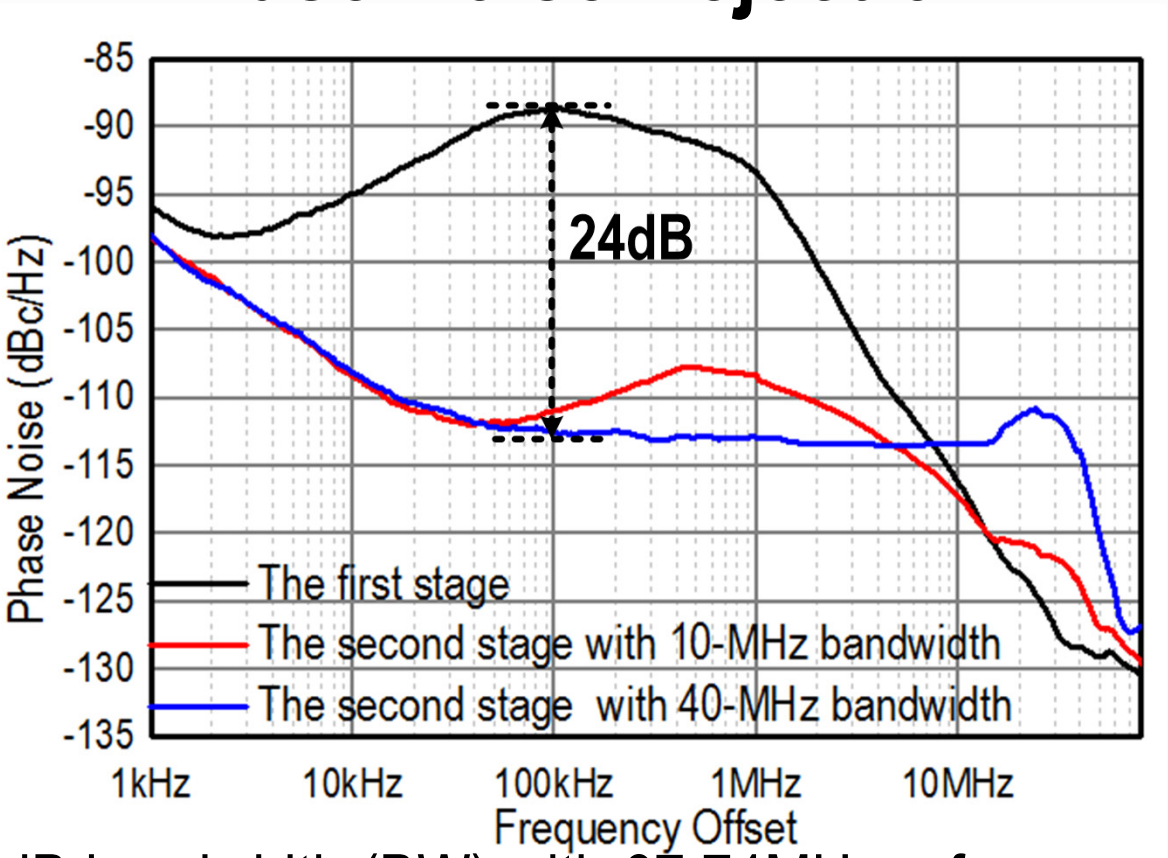


- 65nm CMOS with 0.043mm^2 core chip area
  - **0.01mm^2 sub-sampling DLL**
- Supply voltage: 1.2V
- Total power of 3.84mW:
  - PLL : 2.88mW
    - VCO: 1.56mW
    - PLL loop: 1.32mW
  - **Sub-sampling DLL: 0.96mW**
    - VCDL: 0.48mW
    - DLL loop & reference buffer: 0.48mW

Outline

- ◊ Motivation
- ◊ Existing PLL Architectures
- ◊ Proposed Wide-Band High-Order Cascaded PLL
- ◊ Proposed Clock-Skew Sub-Sampling Phase Detector
- ◊ **Measurement Results**
- ◊ Conclusions

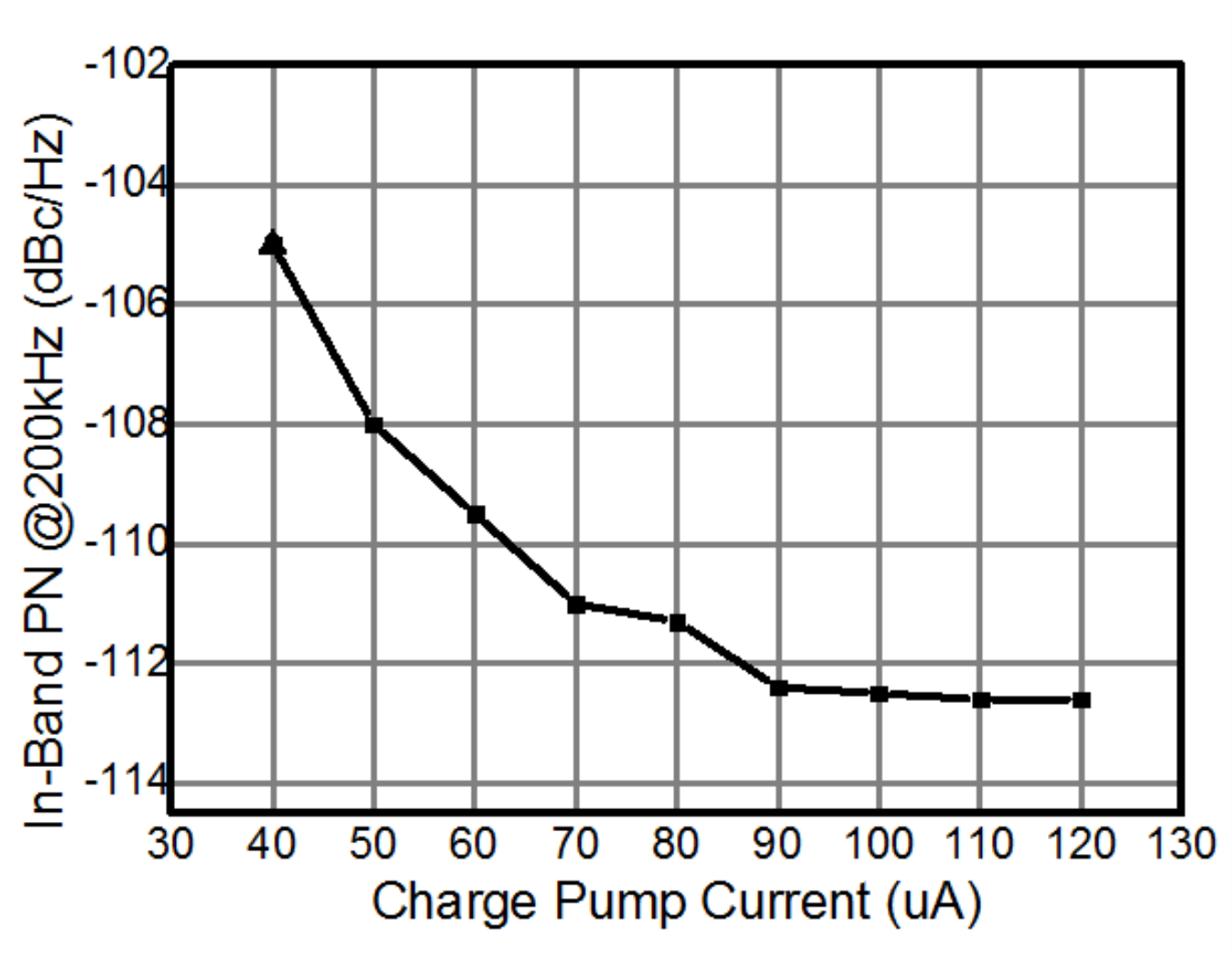
Phase Noise Rejection



- ~40 MHz -3dB bandwidth (BW) with 67.74MHz reference
  - 24dB PN rejection with ¼ extra power consumption
  - 60dB/dec PN rejection→ no need higher-order cascaded PLL for PN rejection
- ~10 MHz BW for optimal loop bandwidth

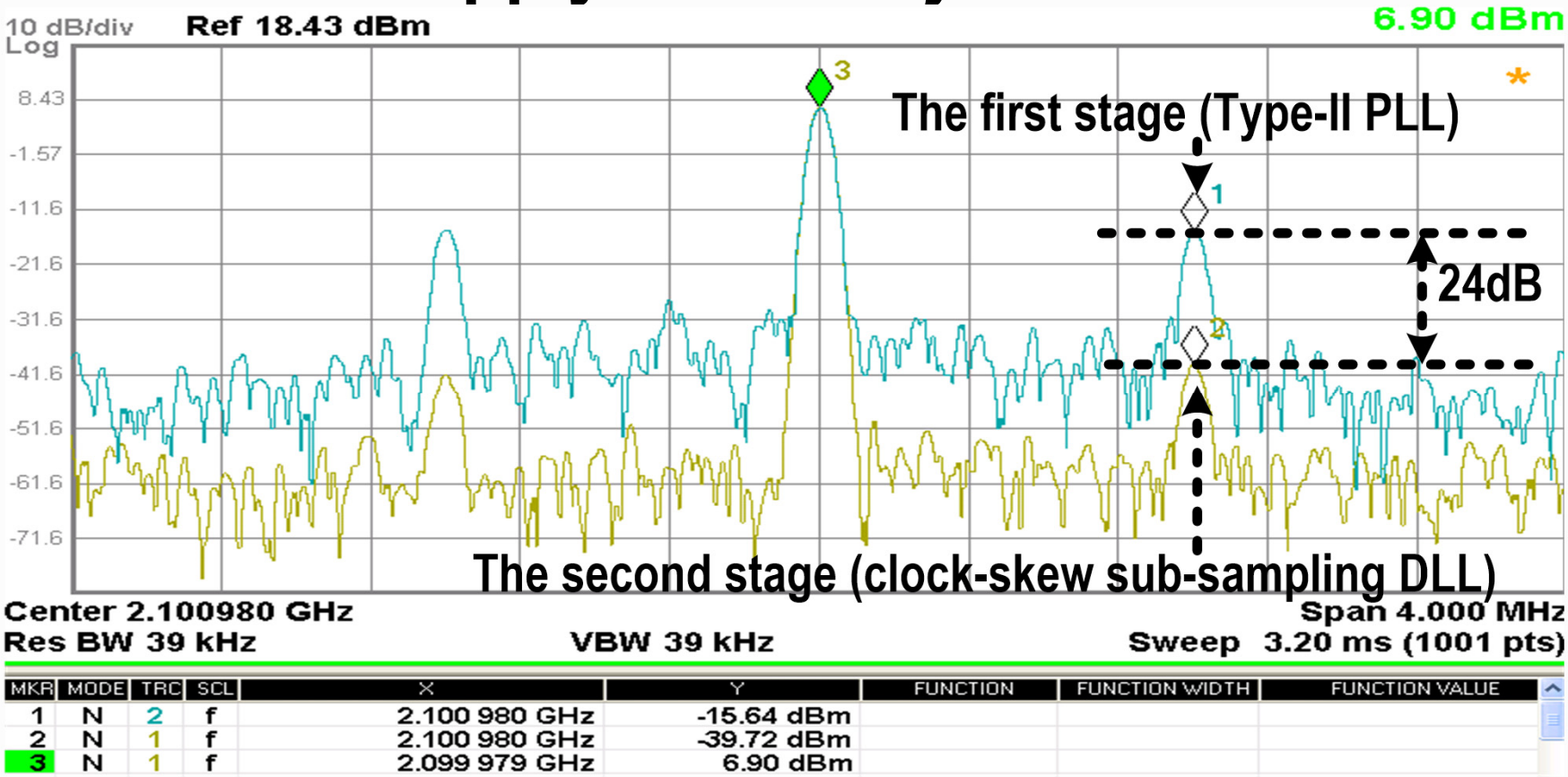
  →integrated jitter suppressed from 3.67ps to 1.05 ps

In-Band Phase Noise



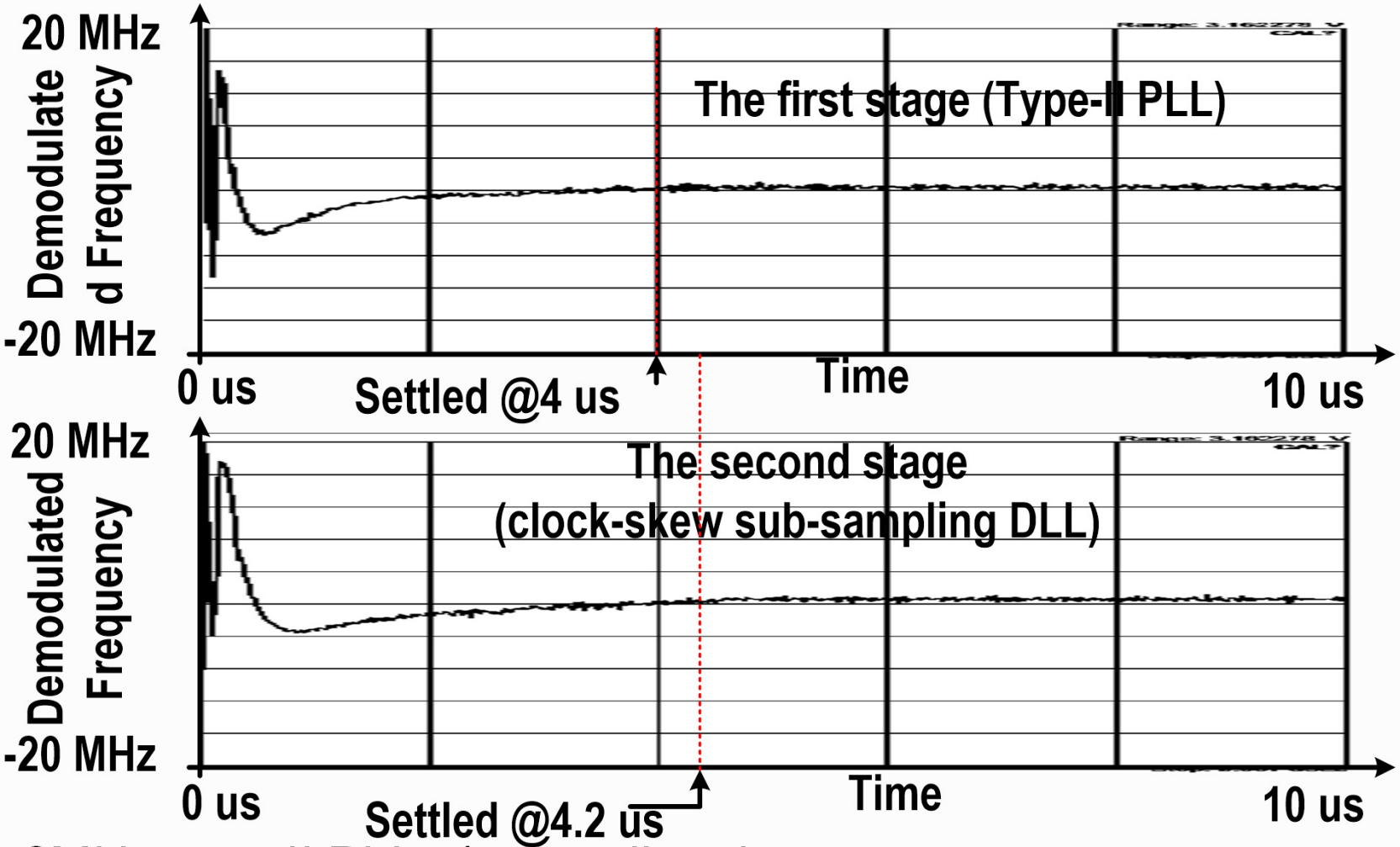
◊ 90uA total charge-pump current → -112.6dBc/Hz in-band phase noise

Supply Noise Rejection



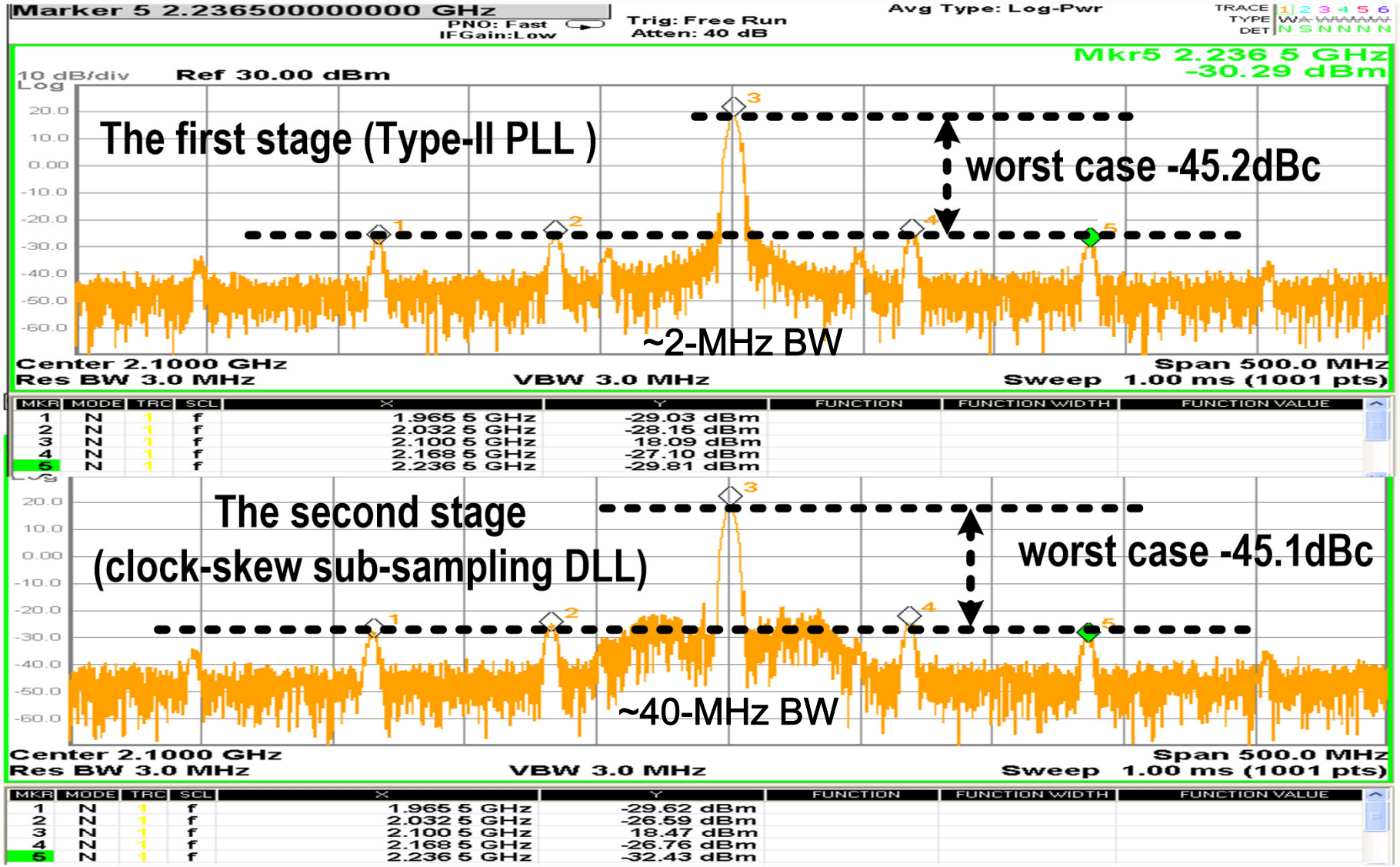
- Inject -74dBm 1MHz to VCO's supply → periodic frequency drift
  - →w/o the second stage: -22dB spur due to periodic frequency modulation
  - →with the second stage: -46dB output spur
  - →24dB rejection → Higher-order cascaded PLL for more rejection

Settling Time Measurement



- ~2MHz type-II PLL: 4us settling time
- ~40MHz clock-skew sub-sampling DLL: 4.2us settling time

Reference Spur Measurement



◊ 0.1dB reference spur degradation

Performance Summary and Comparison

	A. Sai, ISSCC'12	W. Deng, ISSCC'14	L. Kong, ISSCC15	Y. C. Huang, ISSCC'14	X. Gao, ISSCC''10	This Work	
PLL Architecture	Type-III PLL	IL-PLL	Type-I PLL	ADPLL	Sub-Samp.	Cascaded PLL	
VCO Type	Ring	Ring	Ring	Ring	LC	Ring	
Output Freq.	3.24 GHz	0.9 GHz	2.39 GHz	2.418 GHz	2.21 GHz	2.1 GHz	
Freq. Tuning Range	1.4-3.2 GHz	0.39-1.41 GHz	2.0-3.0 GHz	N/A	N/A	1.1-2.1 GHz	
Ref. [MHz]	108	150	22.6	26	55.25	67.74	
Multi. Ratio	30	6	106	93	40	31	
In-band PN [dBc/Hz]	-110	N/A	-114	-94	-121	-112	-113
Integrated Jitter	1.01ps	1.7ps	0.97ps	3.3ps	0.3ps	1.05ps (10MHz)	1.7ps (40MHz)
Power [mW]	27.5	0.78	4	6.4	3.8	3.84	
FOM* [dB]	-225.5	-236.5	-234.2	-223.5	-245	-234	230
Settling Time	85 us	N/A	N/A	N/A	N/A	4.2 us	
Supply Rejection	15dB@2KHz	N/A	N/A	N/A	N/A	15dB *** @1MHz	24dB @ 1MHz
Ref. Spur	N/A	-41dBc	-65dBc	-75dBc	-80dBc	-45dBc	
VDD [V]	1.2	0.8	1	1.1	1.2	1.2	
Core Area [mm^2]	0.32	0.0066	0.015**	0.013	0.2	0.043	
Process	65nm CMOS	65nm CMOS	65nm CMOS	40nm CMOS	180nm CMOS	65nm CMOS	

*FOM=20log(Integrated Jitter/1s)+10log(Power/1mW)

** Active Area ***Extracted from phase noise rejection

Conclusion

- **Cascaded PLL with Sub-Sampling DLL**
  - Break trade-off between loop bandwidth and loop order
    - →~40MHz -3dB bandwidth with 67.74MHz reference and 3rd-order loop
  - Insignificant performance degradation
    - →0.2us degradation to 4us first-stage settling time & 0.1dB degradation to -45.2dBc first-stage reference spur
- **Clock-Skew Sub-Sampling Phase Detector**
  - Extends stable detection range to one reference period
  - Enhanced phase detection gain with time amplifier

Acknowledgement

This project was supported in part by the Hong Kong General Research Funding (16206614) and the National Nature Science Foundation of China (61306030)

A 2-to-16GHz BiCMOS ΔΣ Fractional-N PLL Synthesizer with Integrated VCOs and Frequency Doubler for Wireless Backhaul Applications

Tino Copani, Claudio Asero, Matteo Colombo, Paolo Aliberti, Giuseppe Martino, Francesco Clerici

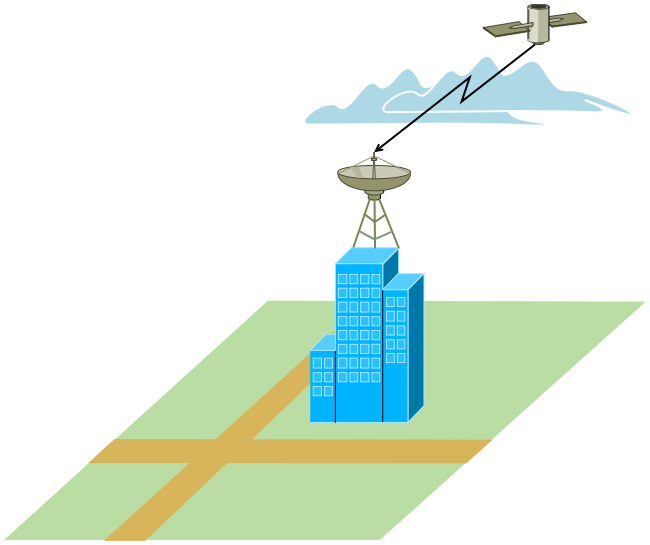
STMicroelectronics, Catania, Italy

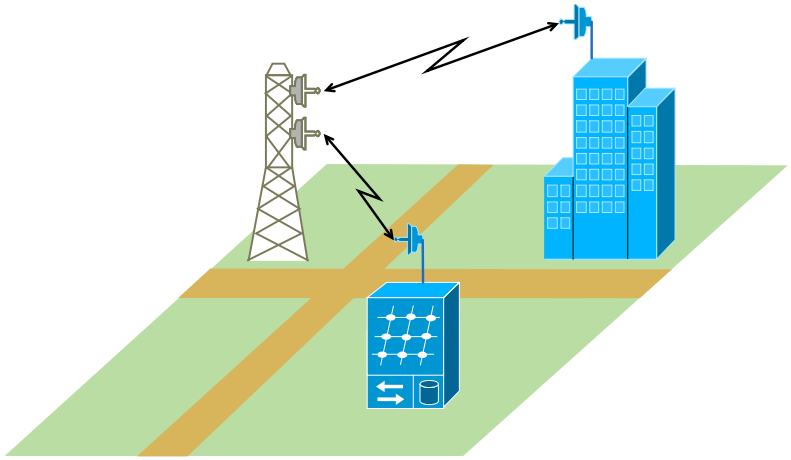
Outline

- Wideband frequency synthesizers overview
- System architecture and challenges
- Block design:
  - Voltage controlled oscillator
  - Frequency doubler
  - High-speed prescaler
- Measurements
- Conclusions

Wideband Frequency Synth. Applications

Satellite Communications





Point-to-point Wireless Backhauls

- Ku-band (~**12GHz** downlink), Ka-band (~**20GHz**) wideband satellite communications
- LoS (line-of-sight) cellular backhauls in the **7.5 - 15GHz** range
- Short-range automotive **RADAR** applications
- Wireless infrastructures (LTE, 4G basestations) in **L-band**

Millimeter-Wave Synth. Challenges

- Very-low phase noise performance
- Wideband operation (to support multiple freq. allocations)
- Stability over thermal cycles (i.e., outdoor units in remote locations

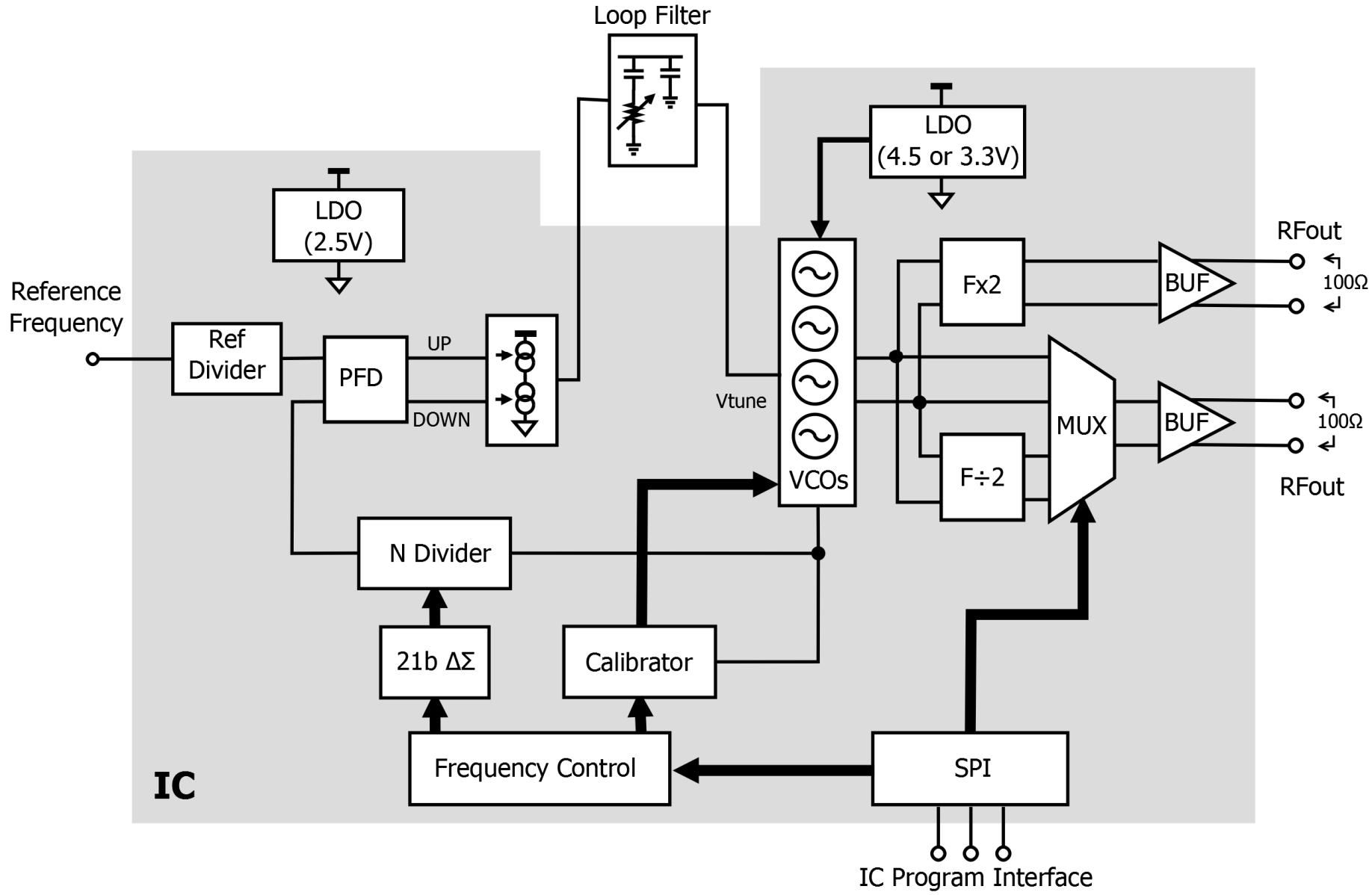
Therefore, so far

✓ Expensive discrete approach (GaAs VCO + PLL IC)

✓ Multiple Local Oscillators (LO) to support different bands on the same unit

✓ High supply voltage

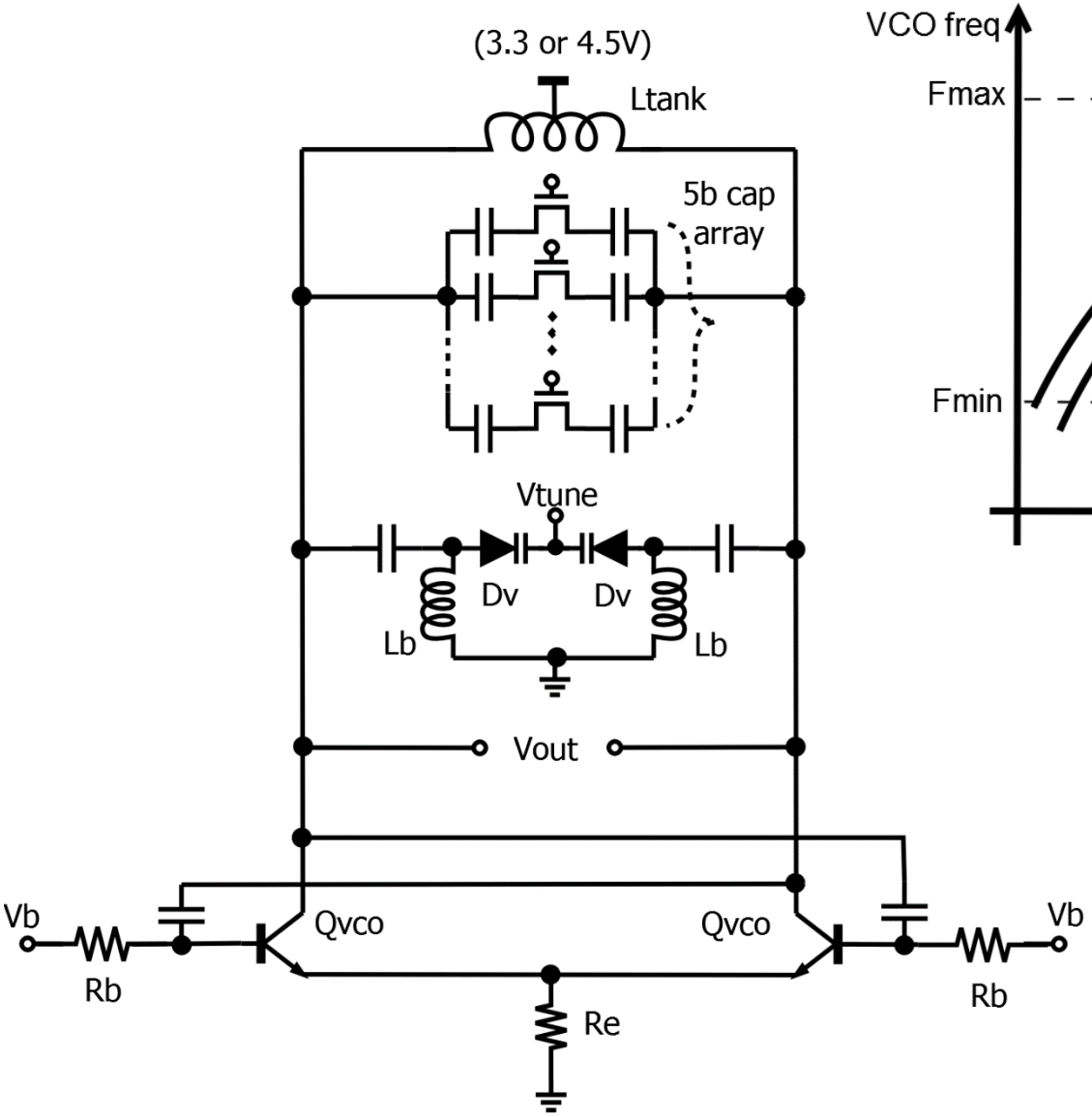
System Architecture

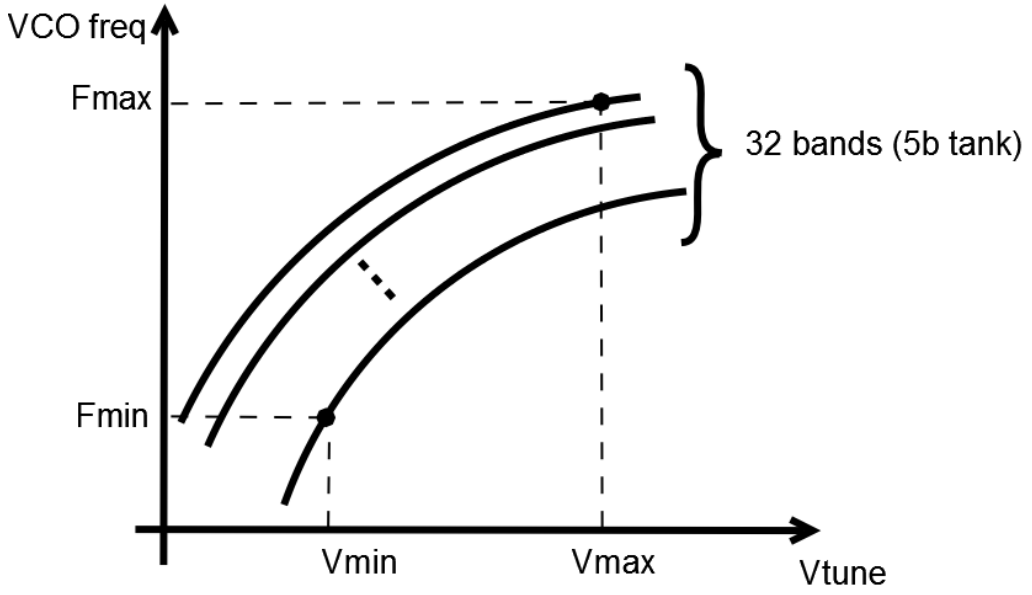


Millimeter-Wave Synth. Features

- ✓ **5b**-tank monolithic VCOs cover **4 – 8GHz**
- ✓ VCO locked over thermal cycle (**-40C** – **+85C**)
- ✓ Integrated frequency doubler (**8 – 16GHz**)
- ✓ Low-noise floor divide-by-2 output (**2 – 4GHz**)
- ✓ Up to **100-MHz** phase comparison frequency (PFD) for low integrated noise
- ✓ Fast-lock through reconfigurable PLL filter
- ✓ On-chip LDO regulators

Voltage Controlled Oscillator Design 1/4





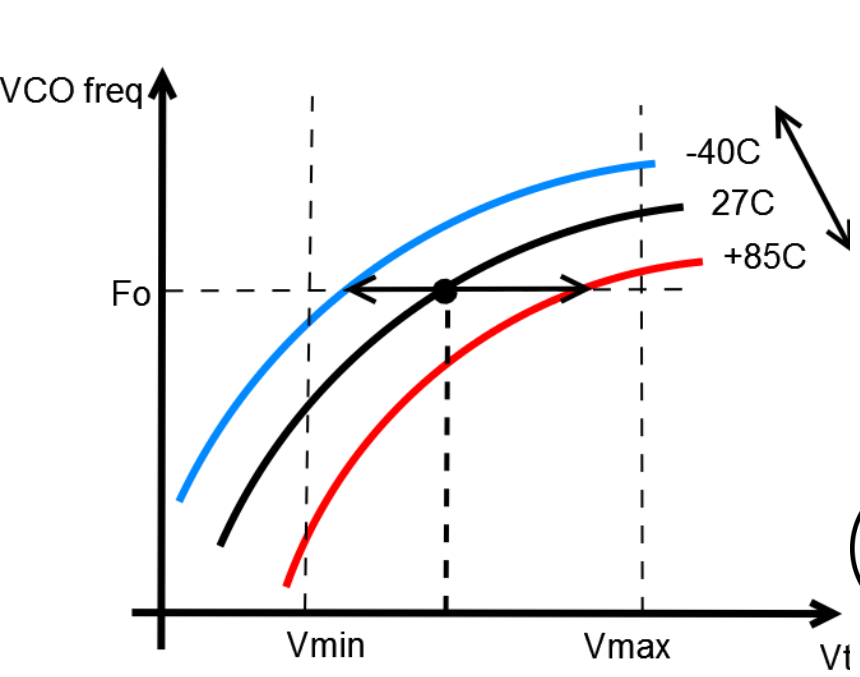
C-class LC tank VCO

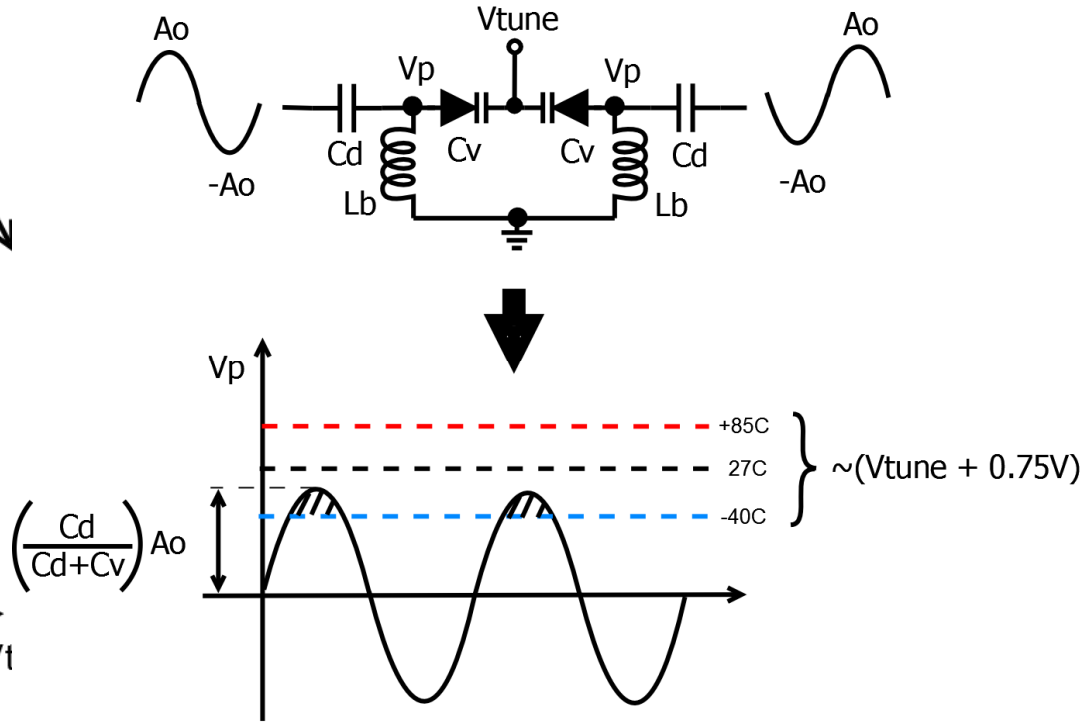
5b capacitor array

3.3 or 4.5V supply

High-swing 4b control (**Vb**)

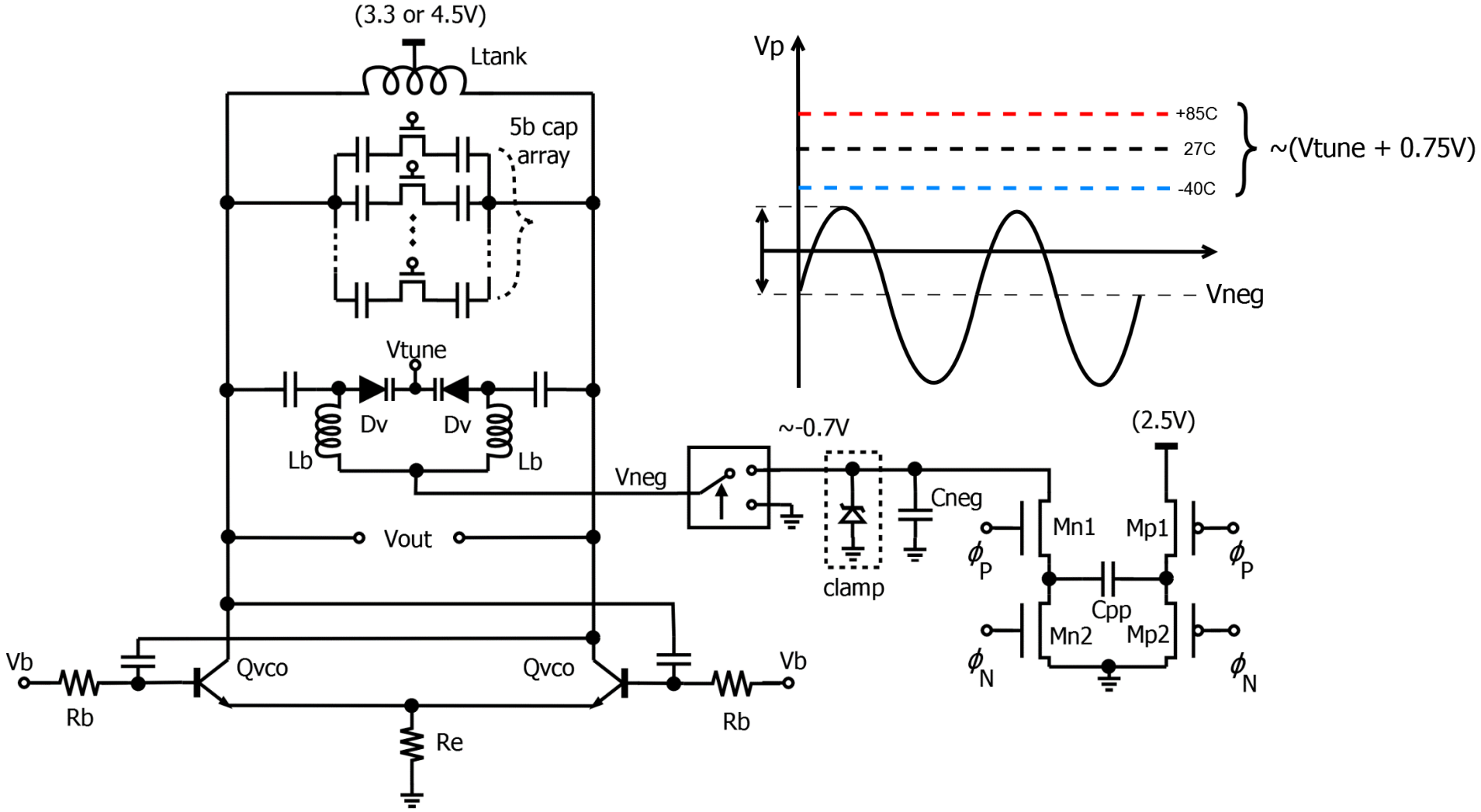
Voltage Controlled Oscillator Design 2/4





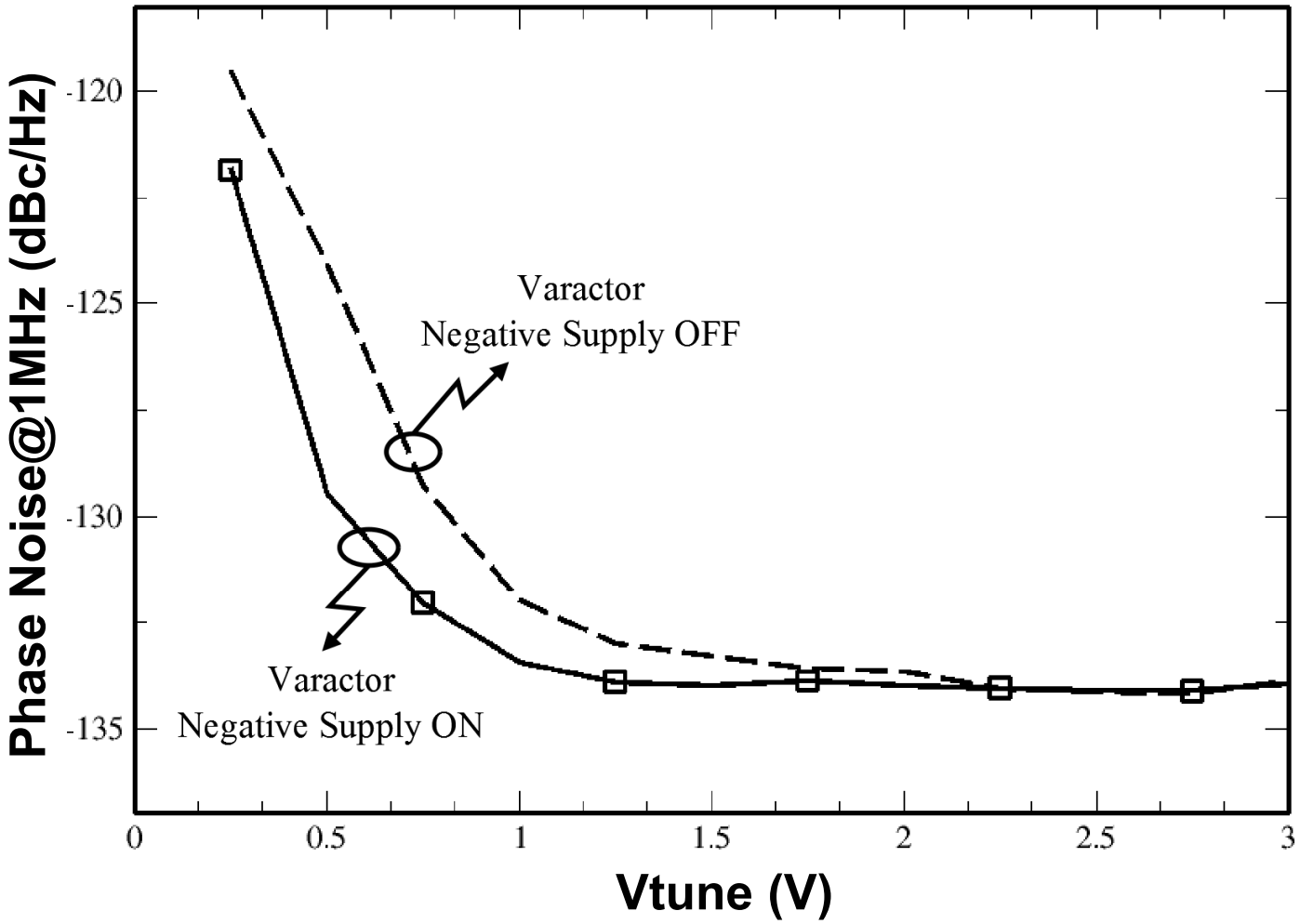
- **Vtune** changes with temperature to maintain PLL lock
- Phase noise increases at low **Vtune** (varactor forward bias)
- Trade-off between thermal stability and VCO swing

Voltage Controlled Oscillator Design 3/4



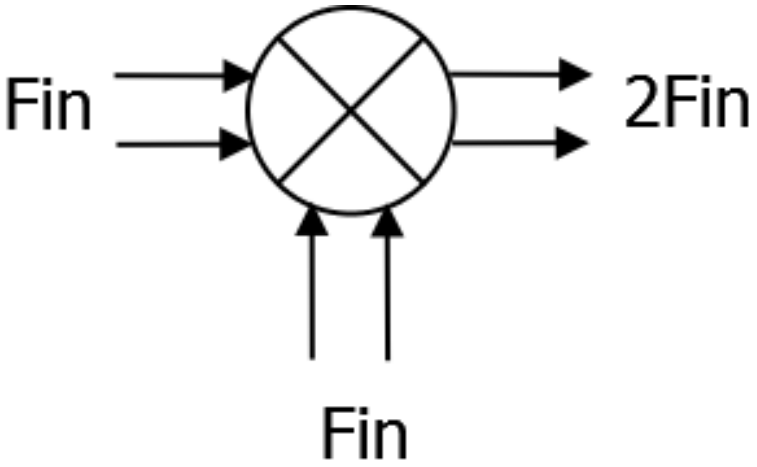
- Negative supply voltage to **Dv** varactor anode
- No **Dv** forward bias at high VCO swing over Temp.

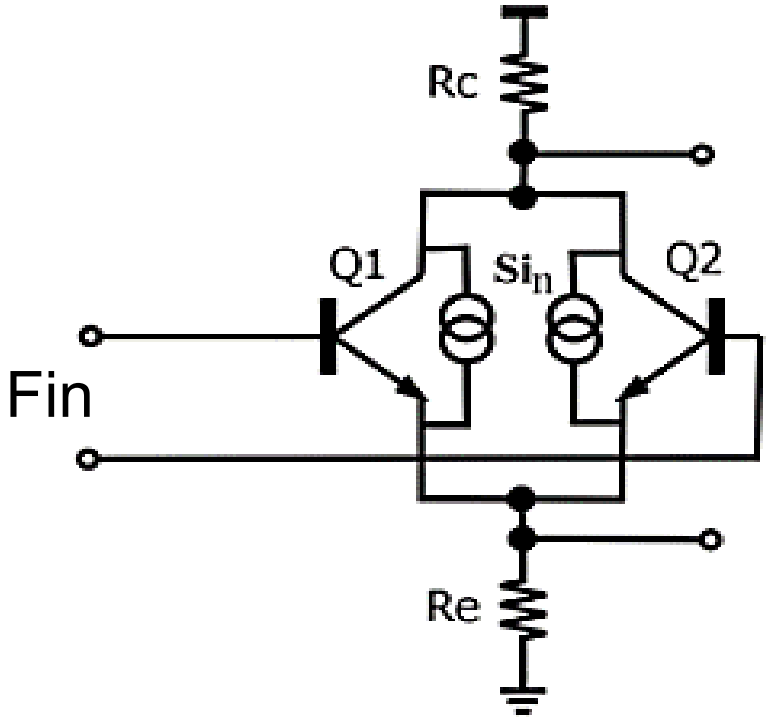
Voltage Controlled Oscillator Design 4/4



- VCO phase noise @**1MHz** from **5GHz** carrier
- Full VCO amplitude for best phase noise

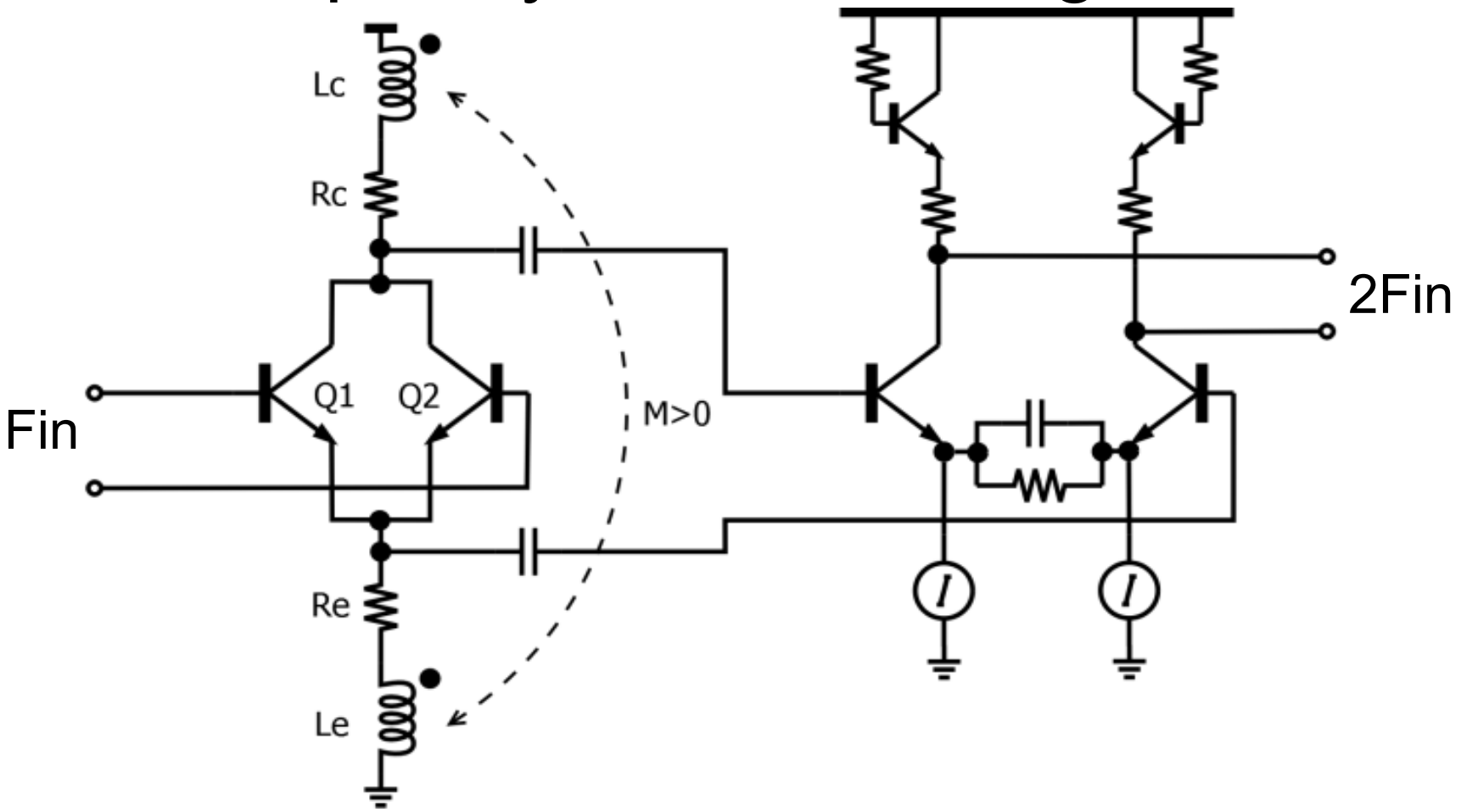
Frequency Doubler Design 1/4





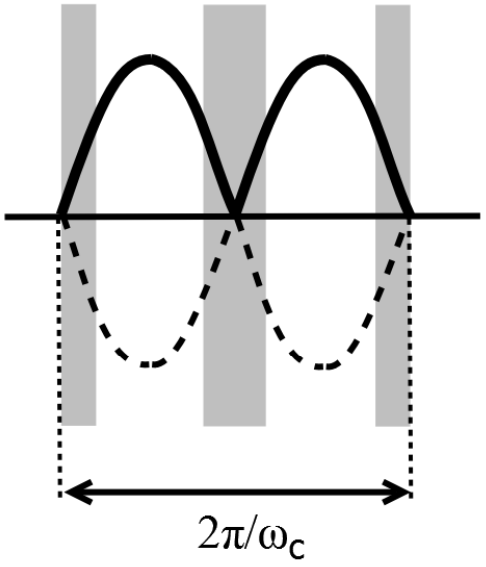
- ✓ Straightforward design
- ✓ Good noise/spur rejection
- ✓ Noisy (device count)
- ✓ High power consumption
- ✓ Low noise
- ✓ Low power
- ✓ Poor spur rejection
- ✓ Differential output imbalance

Frequency Doubler Design 2/4

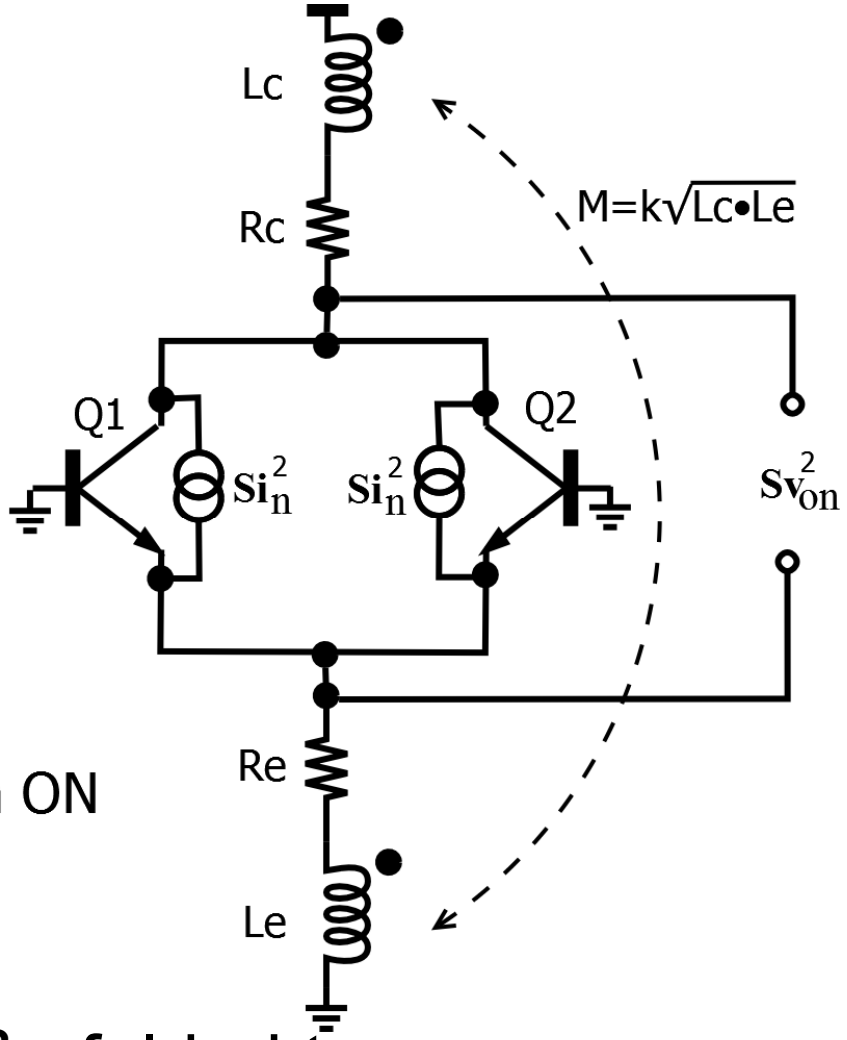


- ✓ Peaking inductors increase bandwidth
- ✓ Inductors' coupling improve output balance, noise, spur rejection

Frequency Doubler Design 3/4



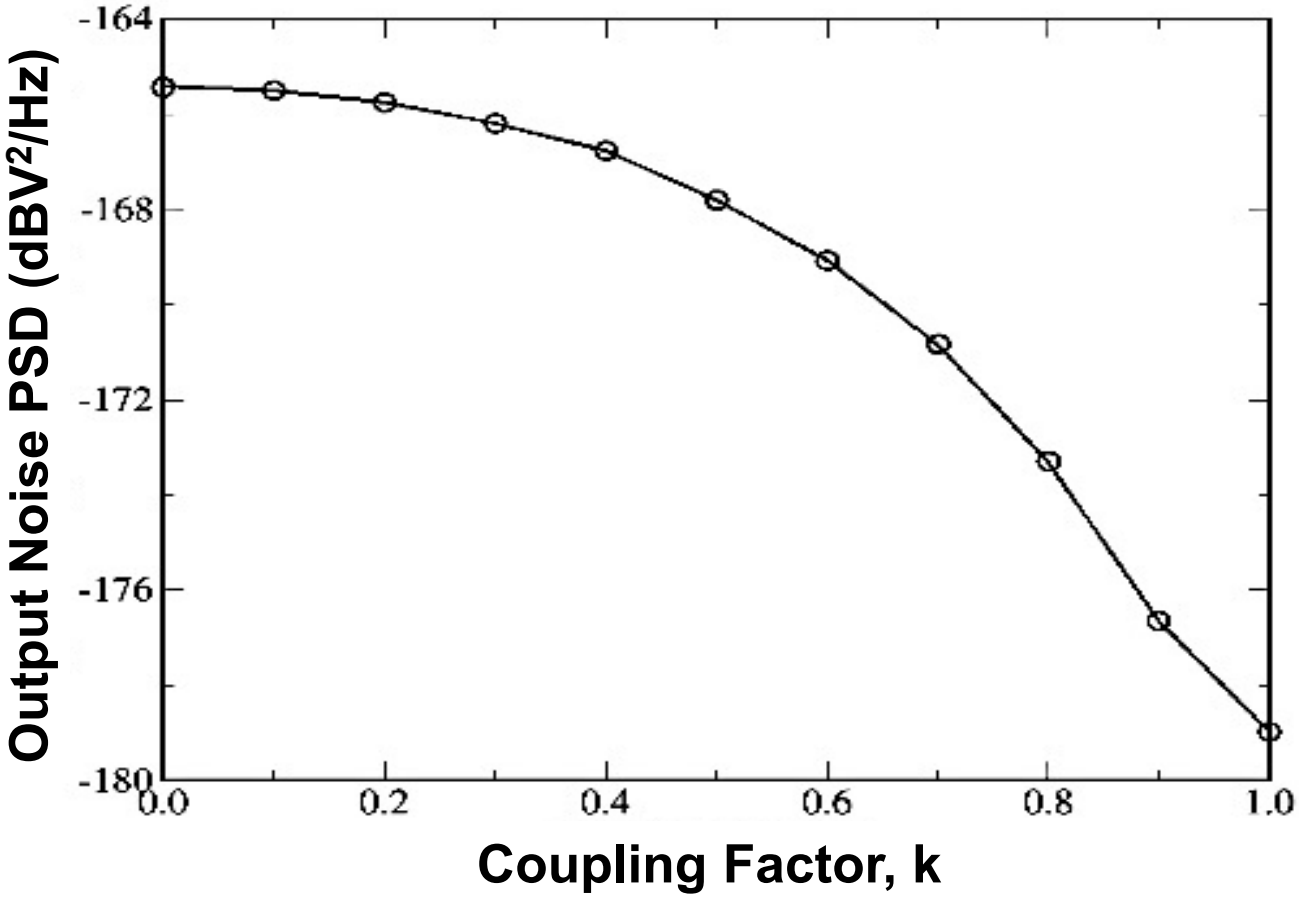
Shaded areas: BJTs are both ON



- **Q1,2** fully switched: $\mathbf{Si^2_n}$ folded to ω_C, $3\omega_C$,…, $(2n+1)\omega_C$
- During transitions: $\mathbf{Si^2_n}$ folded to $2\omega_C$,…, $(2n)\omega_C$

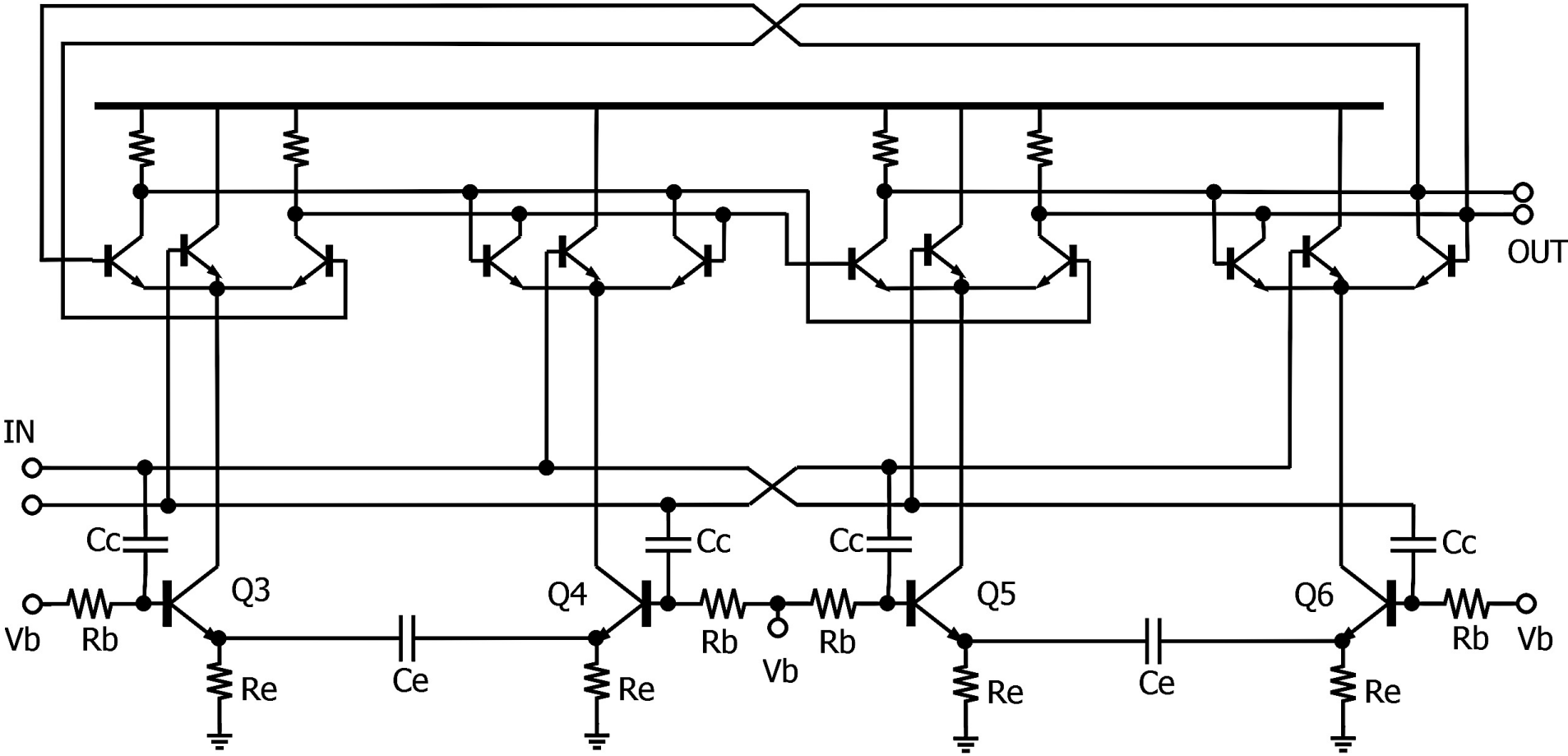
Frequency Doubler Design 4/4

$$S_{V_{on}}^2 = 2qI_C \frac{\left[R^2 + \omega_C^2 L^2 \left(k^2 - 1\right)\right] + 4\omega_C^2 L^2 R^2}{R^2 + \omega_C^2 L^2}$$



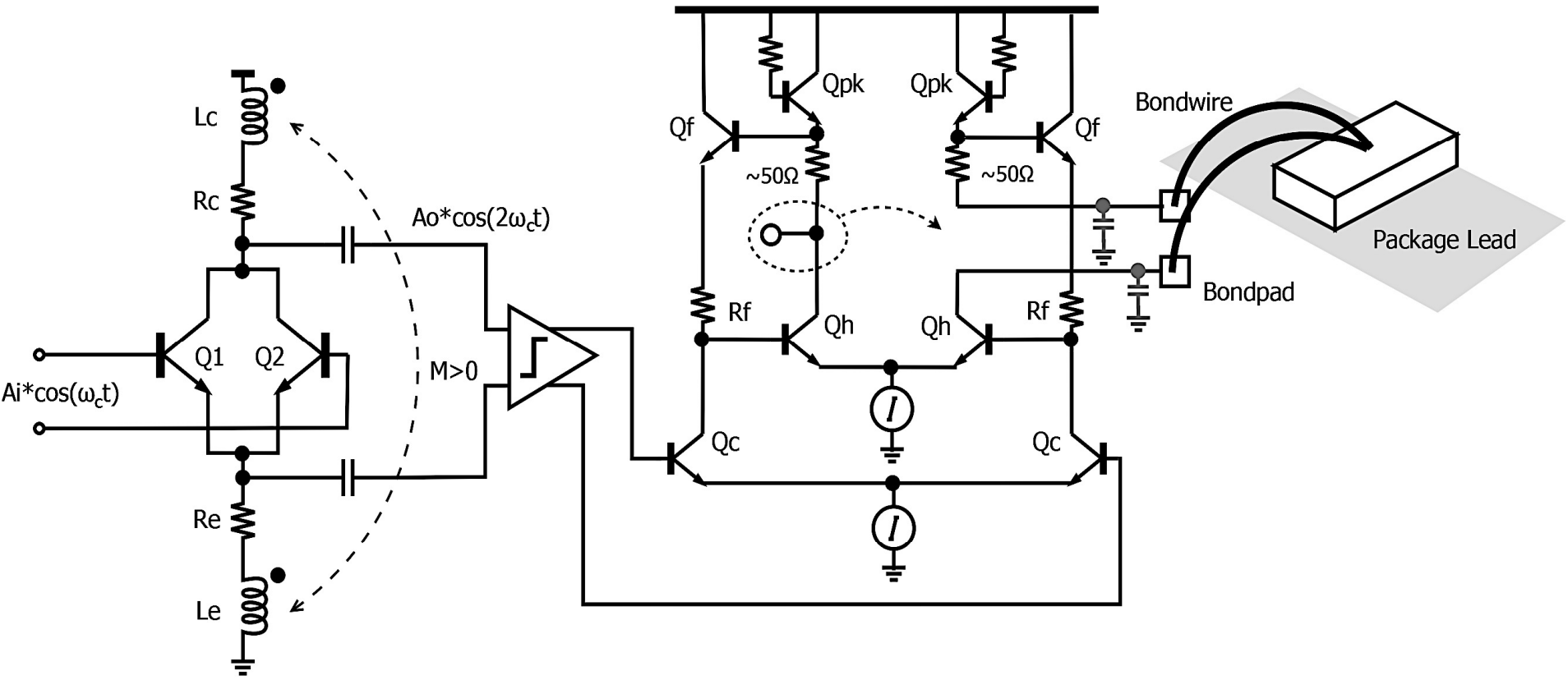
- Coupling, **M=k$\sqrt{\text{LcLe}}$**, reduces device noise impact

Class-AB Divide-by-2 Prescaler



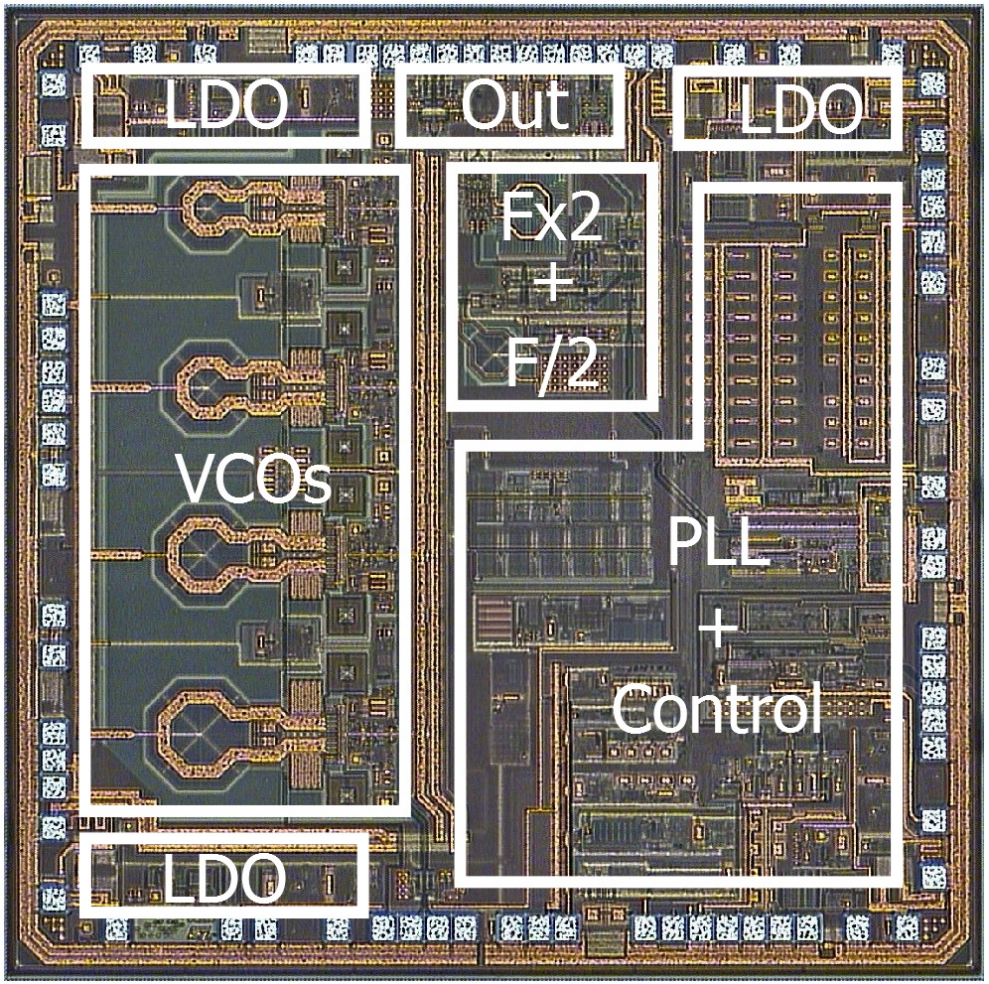
- Triple-tail class-AB latches (**Cc**, coupling capacitors)
- **Re//Ce** latch degeneration

Internally-Matched Output Buffer



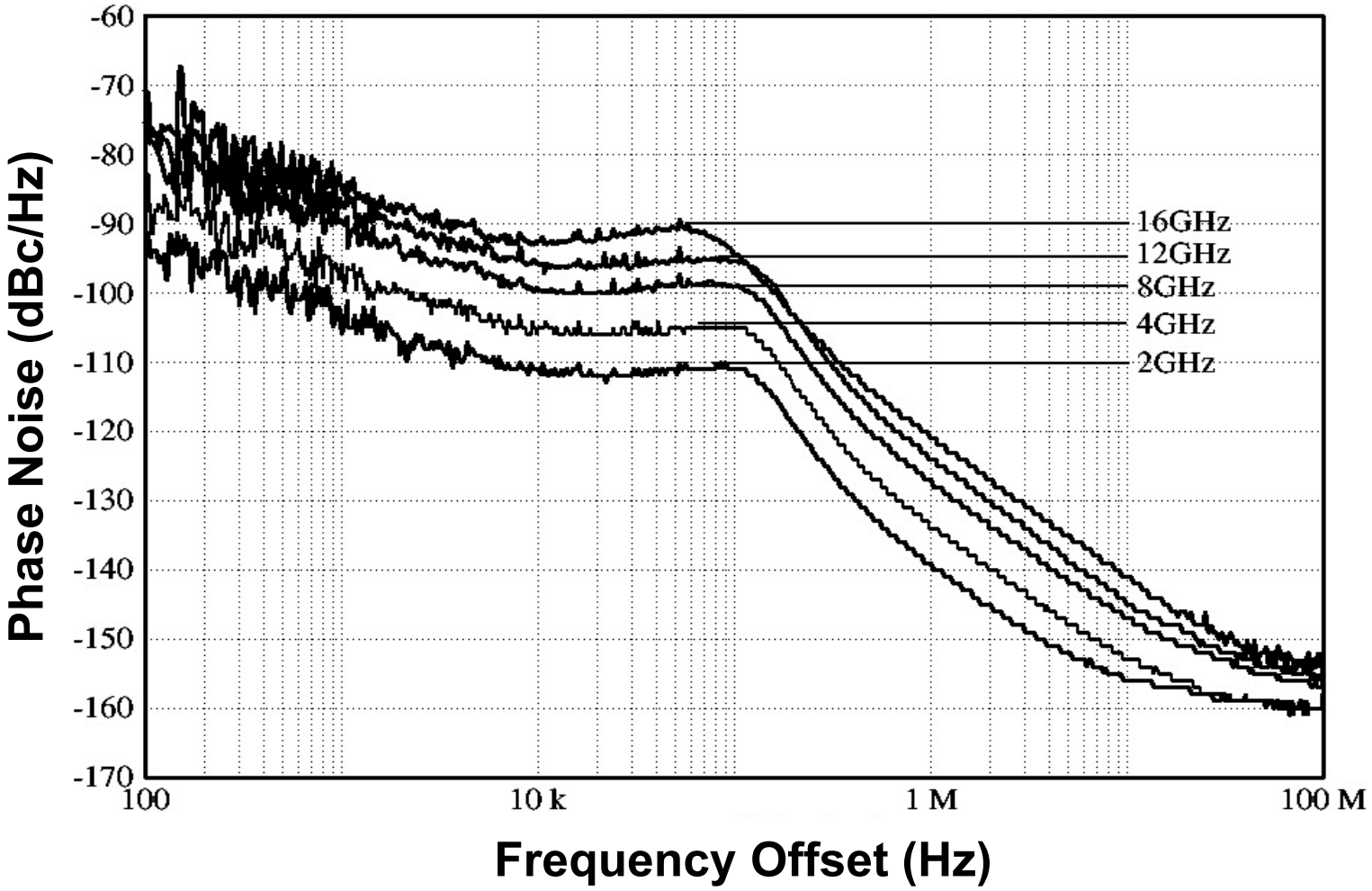
- Modified Cherry-Hooper for broadband operation
- Double-bonding exploited to resonate parasitic caps

IC Fabrication



- **BiCMOS** tech.
- 55-GHz f*t*
- Thick-Cu top metal layer
- MIM capacitors
- **36**-pin **6x6mm^2** QFN package

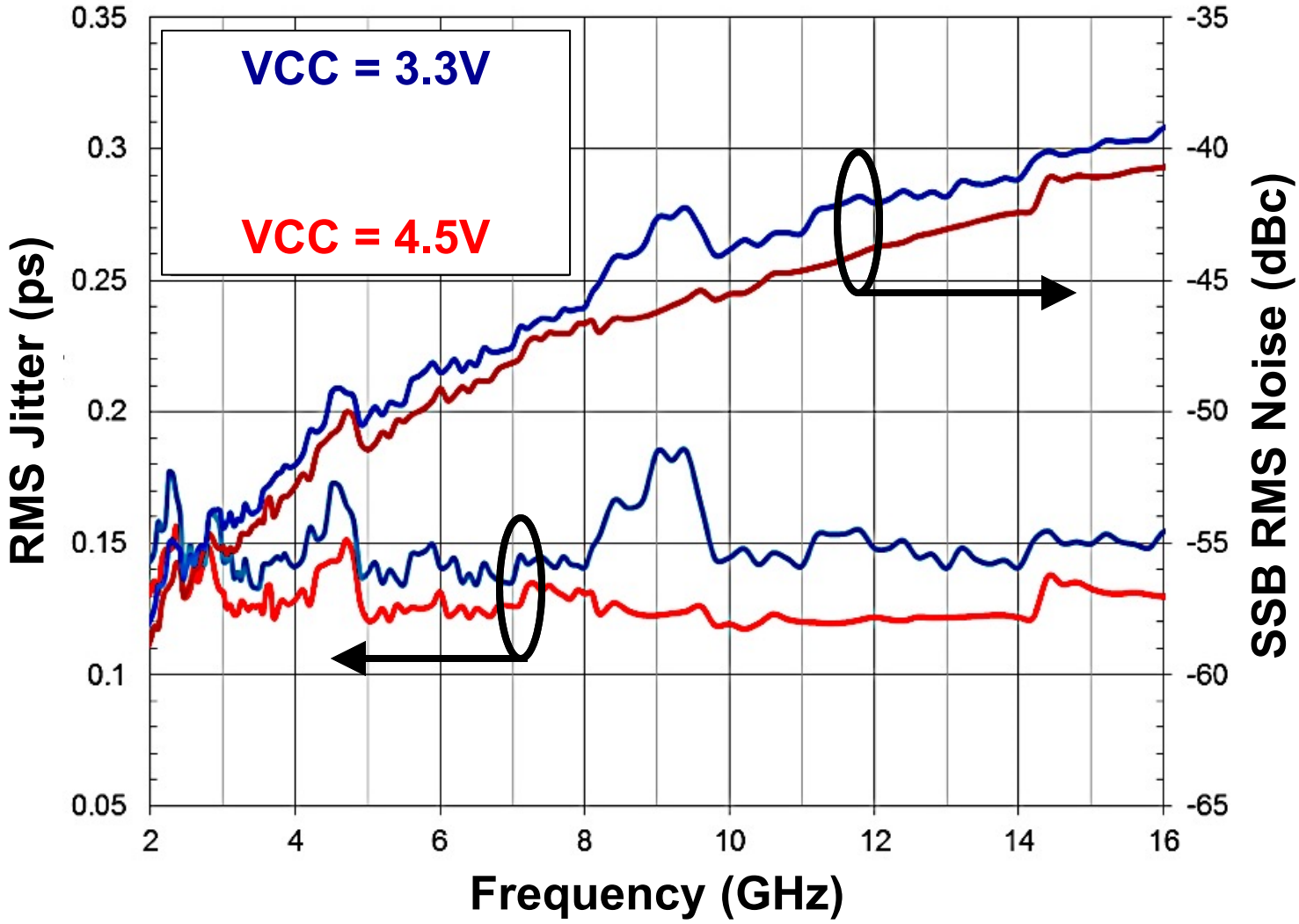
Phase Noise Performance 1/3



- Closed loop noise: **-135dBc/Hz @1MHz, 4GHz**

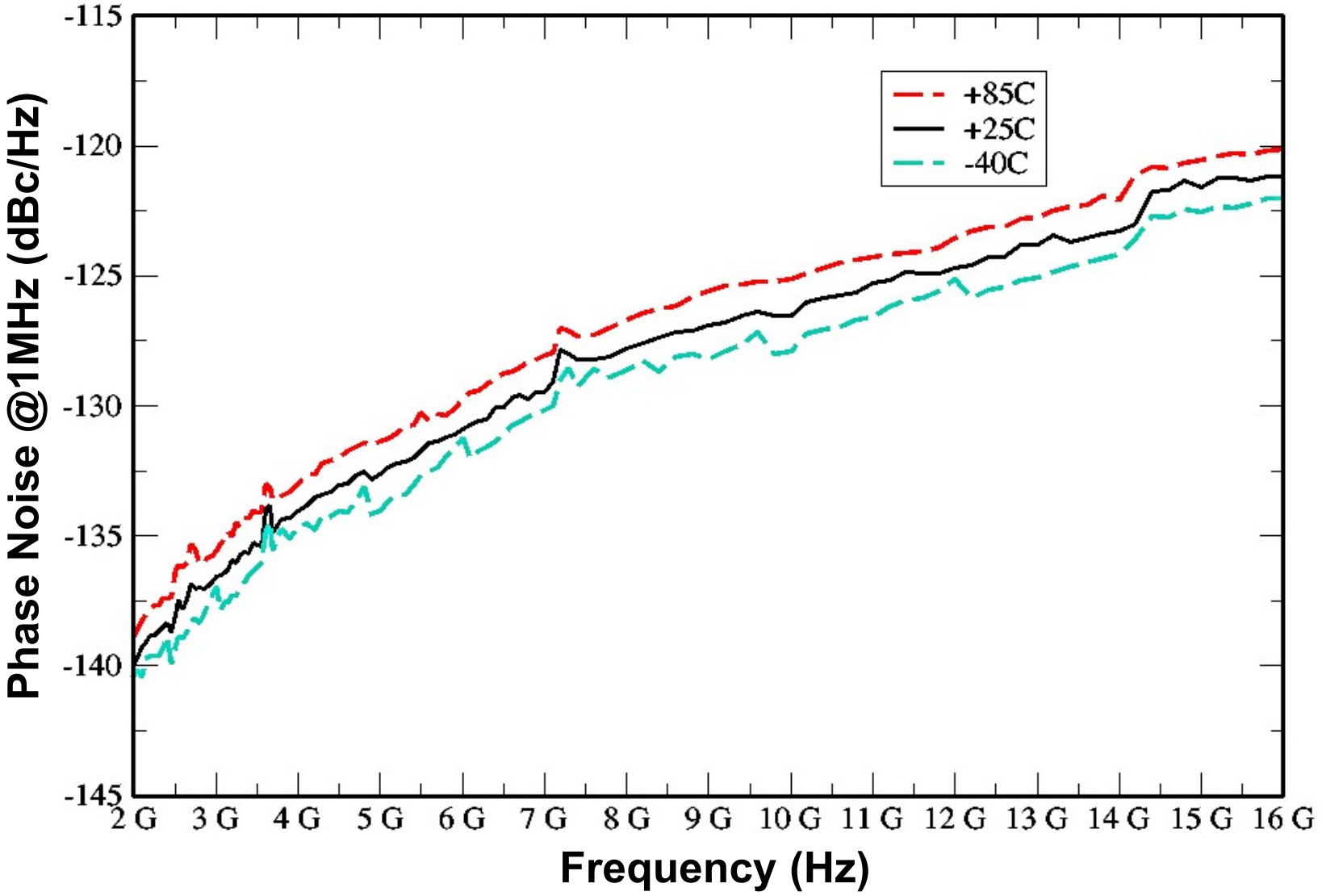
  -122dBc/Hz @1MHz, 16GHz

Phase Noise Performance 2/3



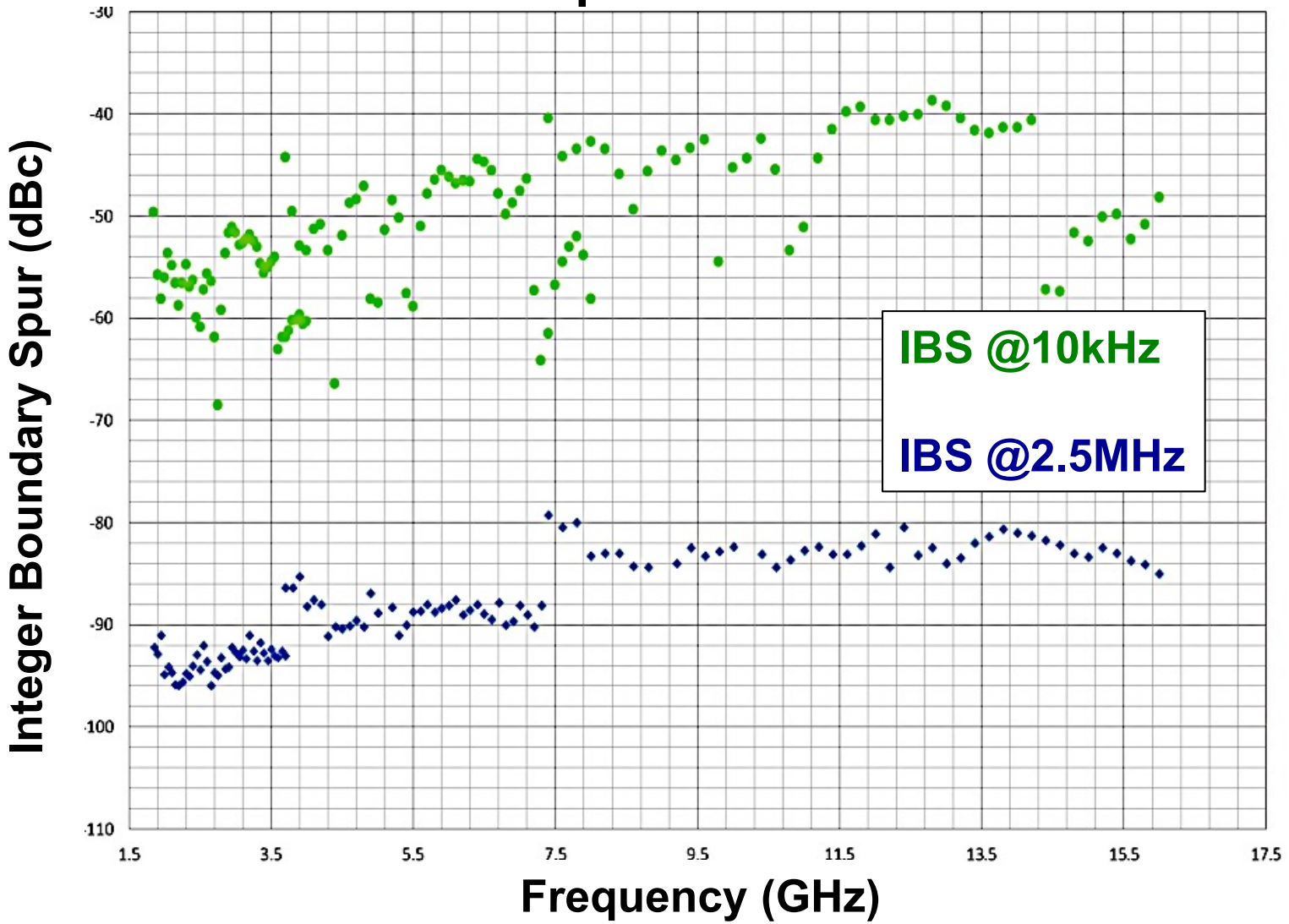
- **SSB** integrated noise at different **supply** voltages

Phase Noise Performance 2/3



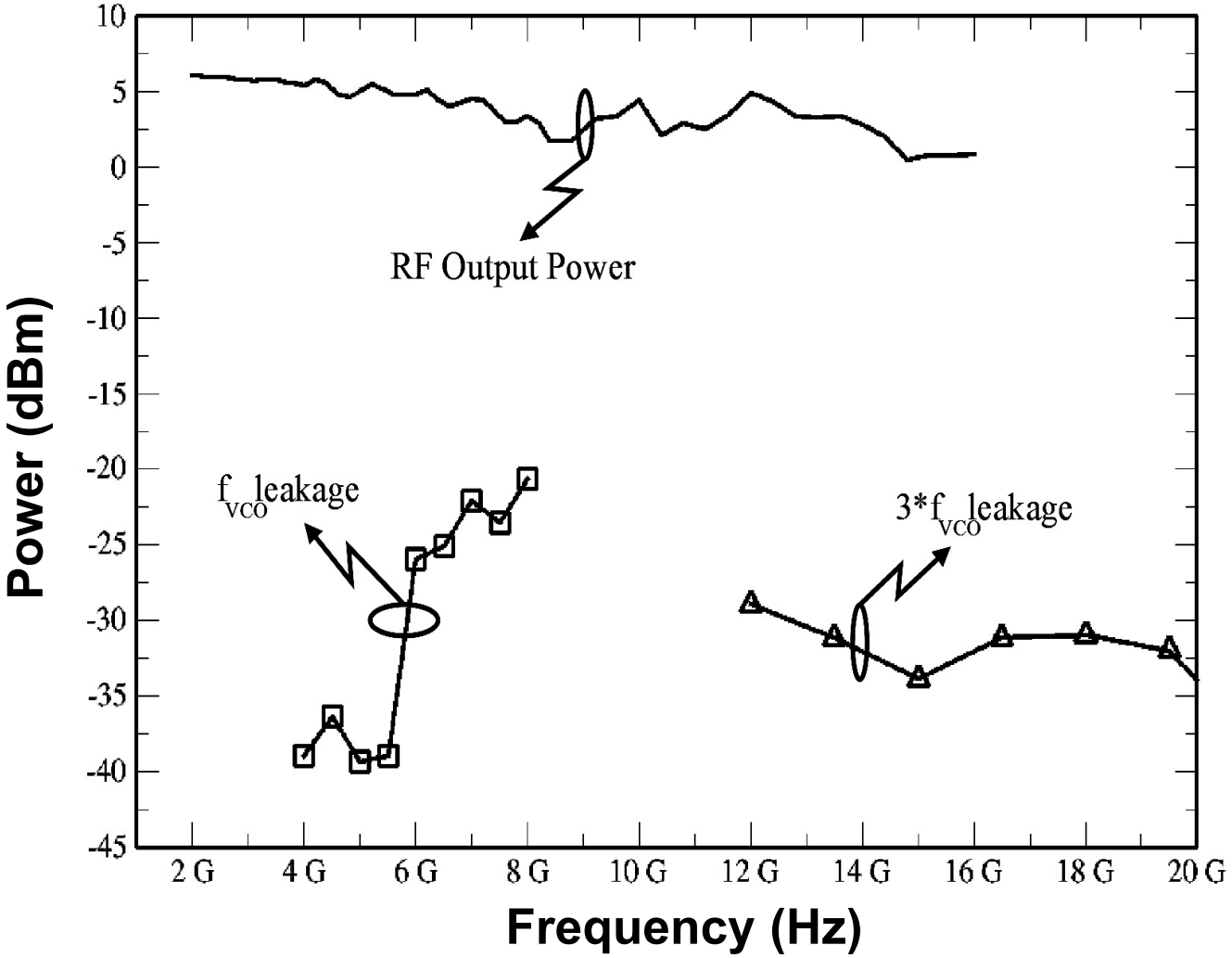
- **±1.25dB** phase noise variation from **-40C** to **+85C**

Fractional Spur Performance



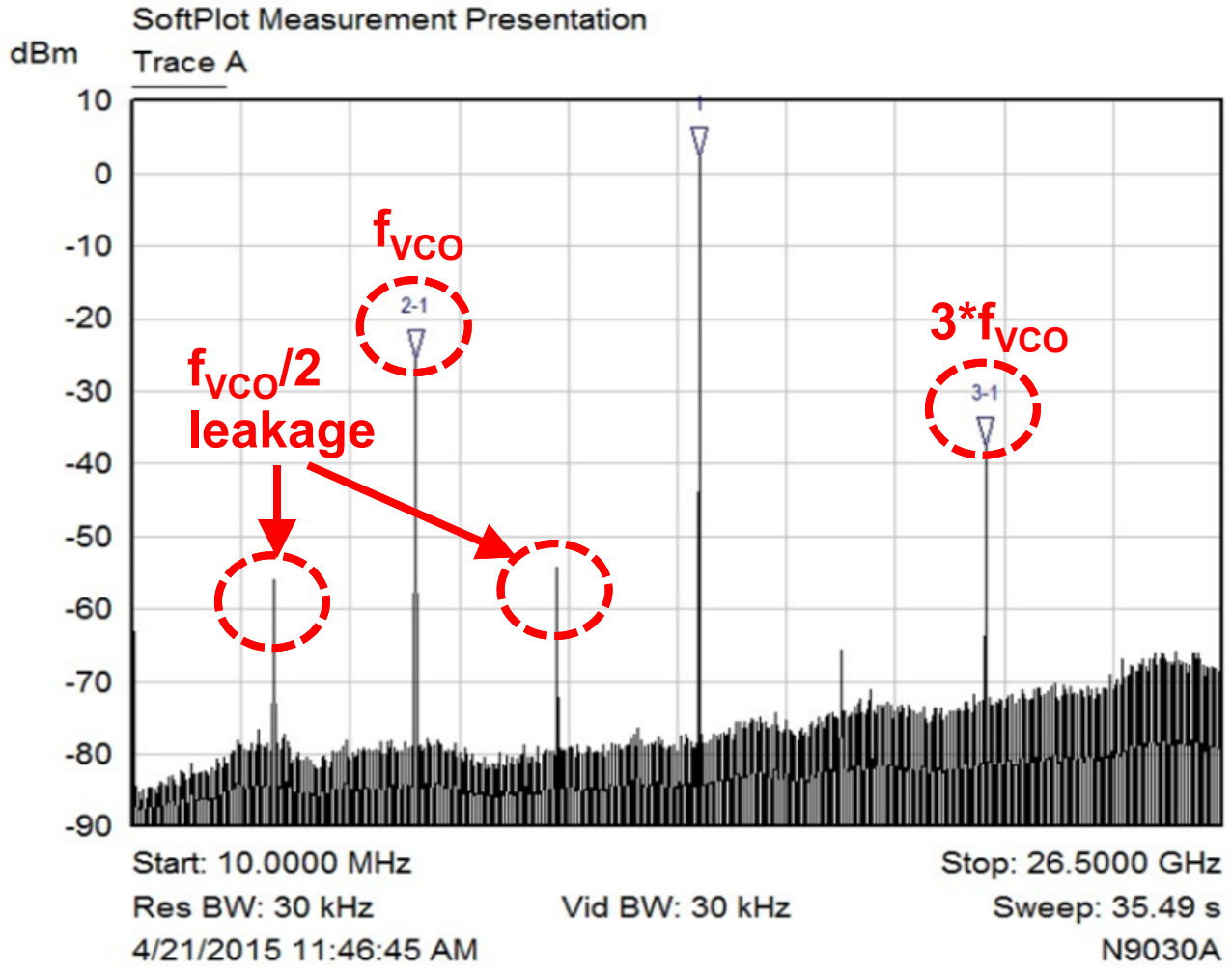
- **10KHz** integer boundary spur below **-40dBc**
- **2.5MHz** integer boundary spur below **-80dBc**

PLL Output Power Measurements



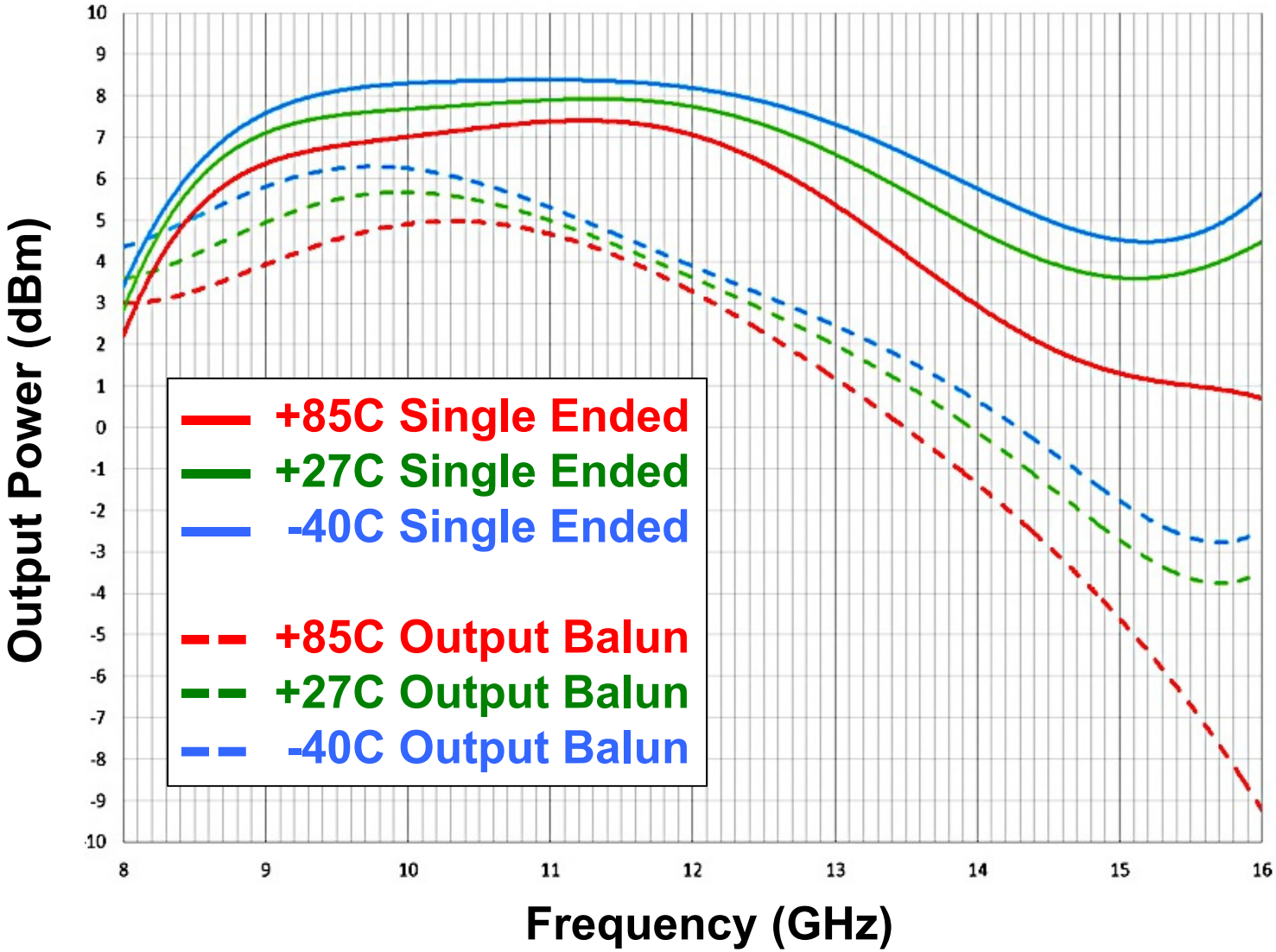
- **+5dBm** output power @**13GHz**
- VCO leakage at doubler output below **20dBc**

PLL Output Spectra @14GHz



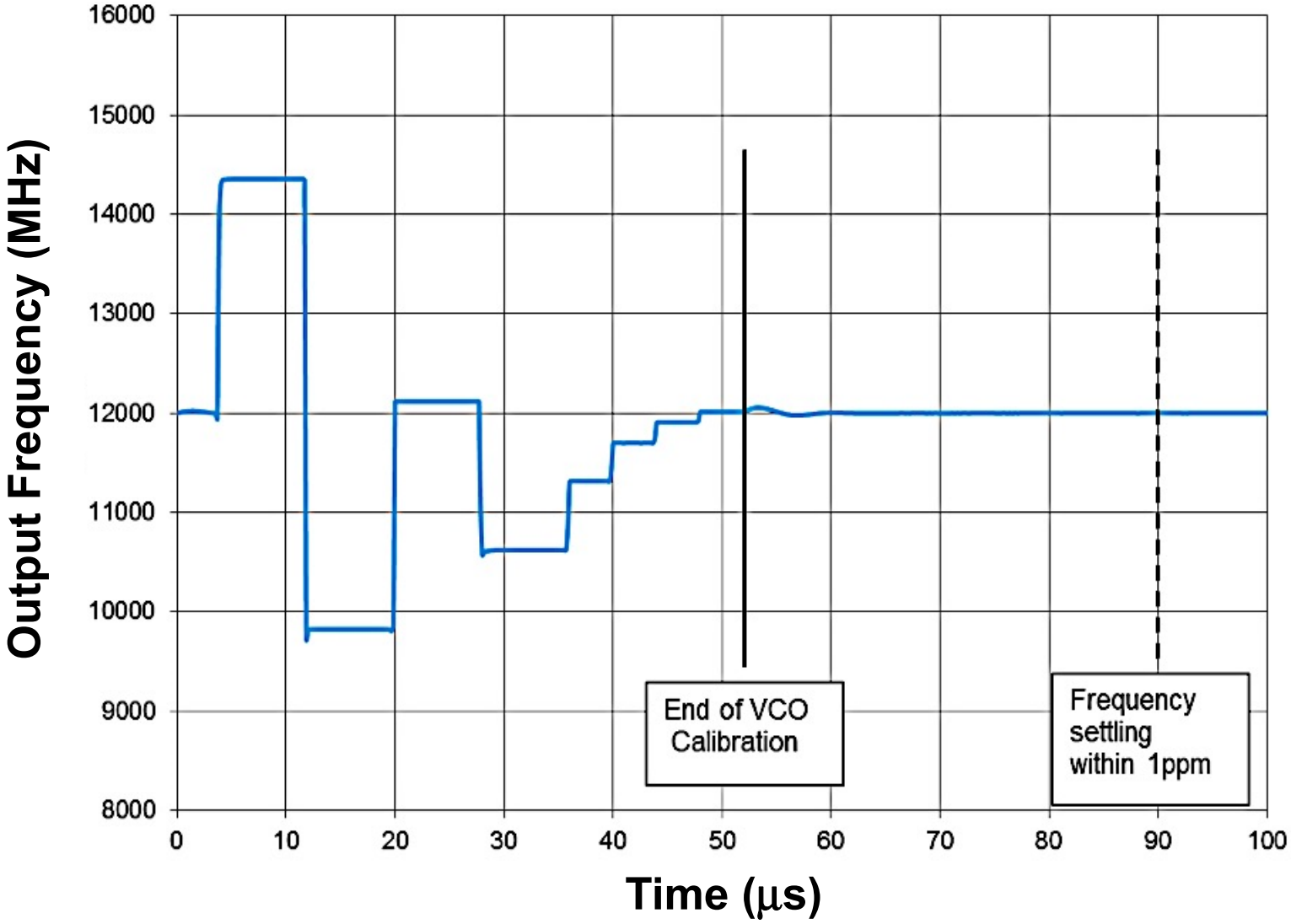
Mkr	Trace	X-Axis	Value	Notes
1	Trace A	13.7848 GHz	2.24 dBm	
2-1	Trace A	-6.8874 GHz	-27.89 dB	
3-1	Trace A	6.9404 GHz	-39.98 dB	

Doubler Output Power vs. Temp



- **±1.5dB** output power @ freq < **13GHz**

PLL Settling Behavior



- **90µs** to settle PLL freq. within 1ppm (BW = **60kHz**)

Comparison against state-of-art designs

Reference	1	2	3	This work
VCO range (GHz)	4 – 8	2.15 – 4.3	20.4 – 27.6	4 – 8
Synth range (GHz)	0.125 – 26	0.3 – 2.15	0.64 – 4.6 5.1 – 6.9 10.2 – 13.8	2 – 16
PFD freq (MHz)	20	123	25	100
Phase noise @10kHz (dBc/Hz)	-86 (6GHz)	-98 (4GHz)	-105 (3GHz)	-106 (4GHz)
Phase noise @1MHz (dBc/Hz)	-118 (6GHz)	-130 (4GHz)	-122 (3GHz)	-135 (4GHz)
IC consumption (mW)	1283	N/A	680	1116

[1] S. Yu, et al., "A Single-Chip 125-MHz to 32-GHz Signal Source in 0.18-mm SiGe BiCMOS," IEEE J. Solid-State Circuits, vol. 46, pp. 598-614, March, 2011.

[2] M. P. Kennedy, et al., "0.3–4.3 GHz Frequency-Accurate Fractional-N Frequency Synthesizer with Integrated VCO and Nested Mixed-Radix Digital Δ–Σ Modulator-Based Divider Controller," IEEE J. Solid-State Circuits, vol. 49, pp. 1595-1605, July, 2014.

[3] S. A. Osmany, et al., "An Integrated 0.6–4.6 GHz, 5–7 GHz, 10–14 GHz, and 20–28 GHz Frequency Synthesizer for Software-Defined Radio Applications," IEEE J. Solid-State Circuits, vol. 41, pp. 1657-1668, September, 2010.

Conclusions

- Widest range low-noise synth. for wireless backhauls
- Innovative design techniques to meet challenging requirements (phase noise, thermal stability, spurs, etc.)
- IC delivers state-of-art performance
- BiCMOS tech. can replace discrete GaAs solutions in the demanding millimiter–wave infrastructure market

Broadcom Corporation, Irvine, CA

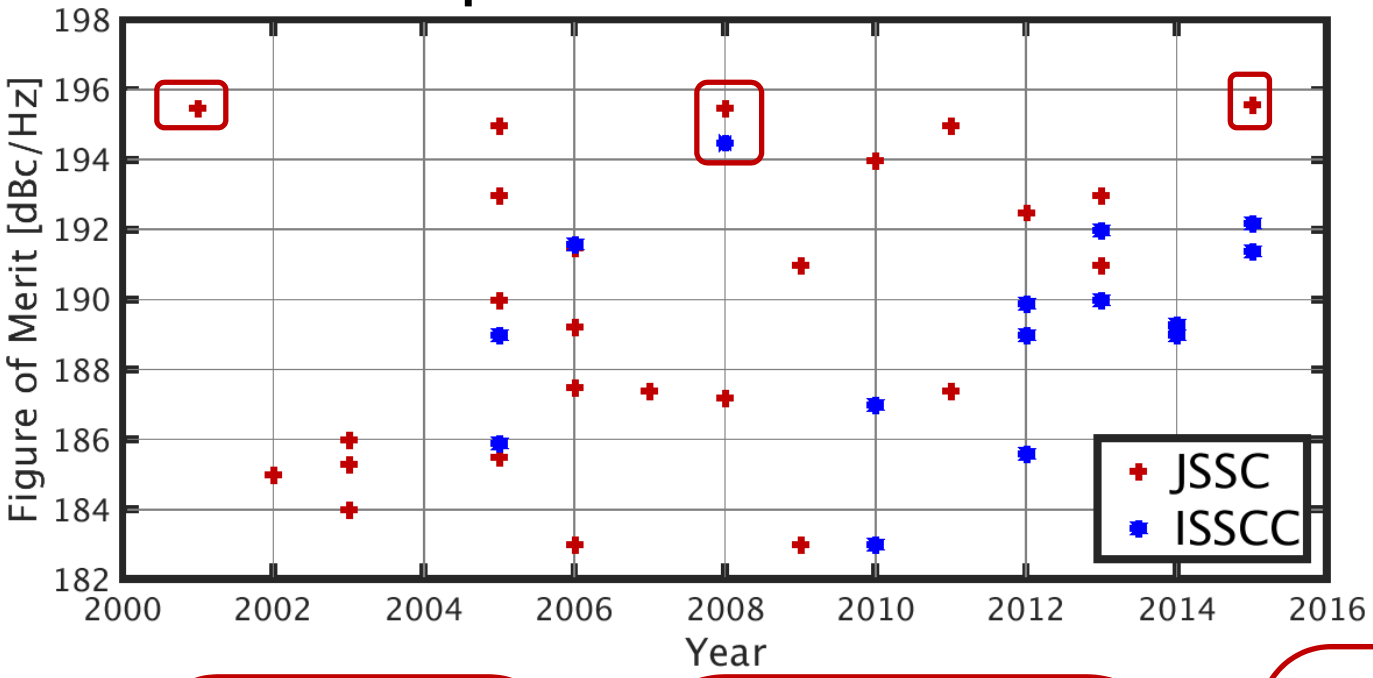
A Complementary VCO for IoE that Achieves a 195 dBc/Hz FOM and Flicker Noise Corner of 200 kHz

David Murphy and Hooman Darabi

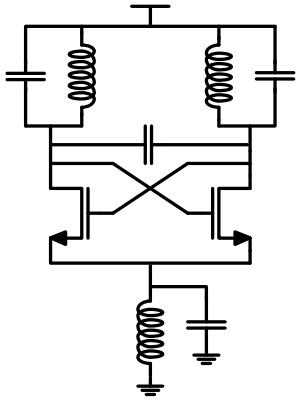
Paper 2.5

2/1/2015

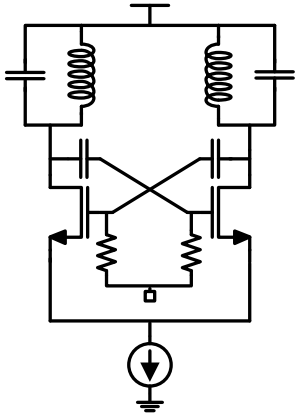
Reported FOMs for LC oscillators



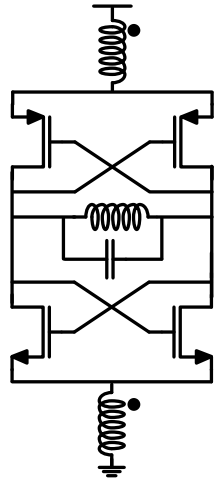
$$FOM = \frac{\left(\frac{\omega_0}{\Delta\omega}\right)^2}{\mathcal{L}_w P_{DC[mW]}}$$



Hegazi & Abidi, *2001.*

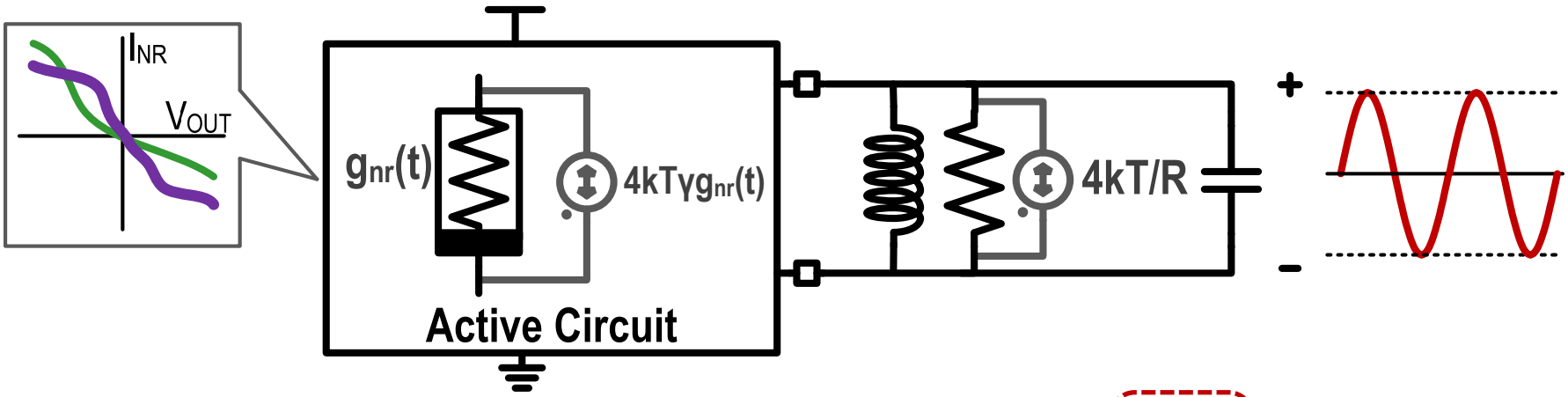


Mazzanti and Andreani, *2008.*



Garampazzi et al, *2015.*

Optimum Figure of Merit



$$FOM\{\Delta\omega\} = \frac{\left(\frac{\omega_0}{\Delta\omega}\right)^2}{\mathcal{L}\{\Delta\omega\}P_{DC[mW]}} = Q^2\frac{\eta}{F}\frac{2}{kT}1\text{m}$$

J. Bank, *Ph.D.*, 2006.
Mazzanti & Andreani, *JSSC*, 2008
Murphy, Rael & Abidi, *TCAS 2012.*
Murphy et al., *CICC 2013*
Mikhemar et al., *JSSC 2013*

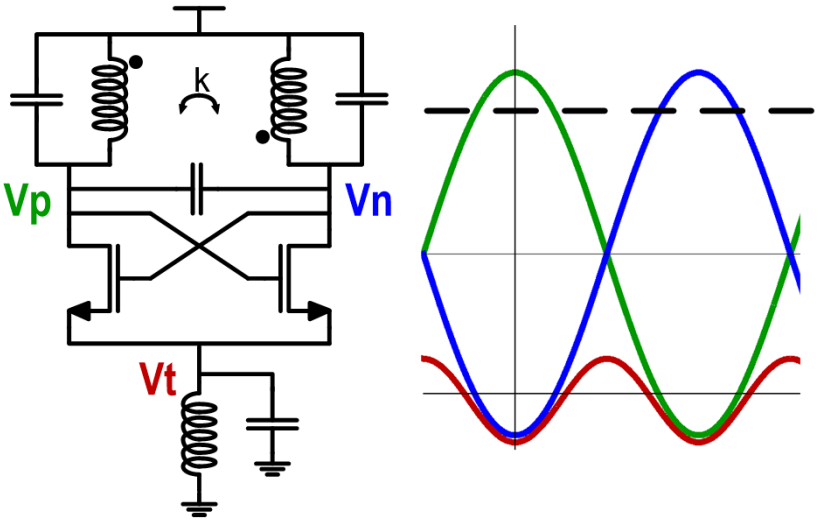
$$\eta_{MAX} = 1$$

$$F_{MIN} = 1 + \gamma \approx 1.67$$

$$FOM_{OPT(dB)} \approx 174.6 + 20\log_{10} Q$$

FOM not expected to improve with time… Q typically doesn't improve with scaling

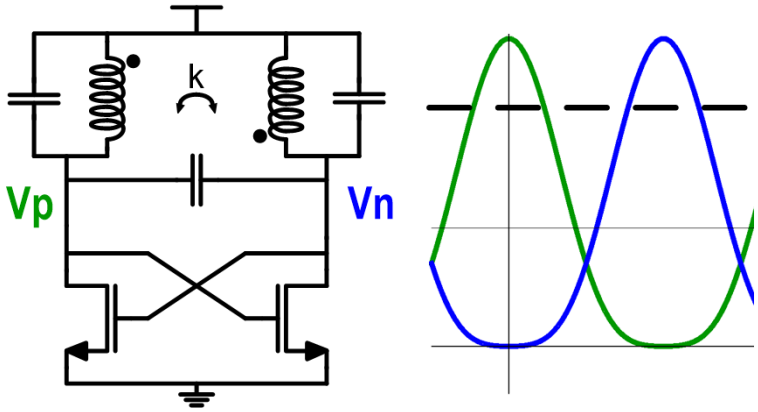
Prior Art: Hegazi's VCO



Hegazi & Abidi. *JSSC 2001.*

$$F = 1 + \gamma$$

$$\eta \approx 80\%$$



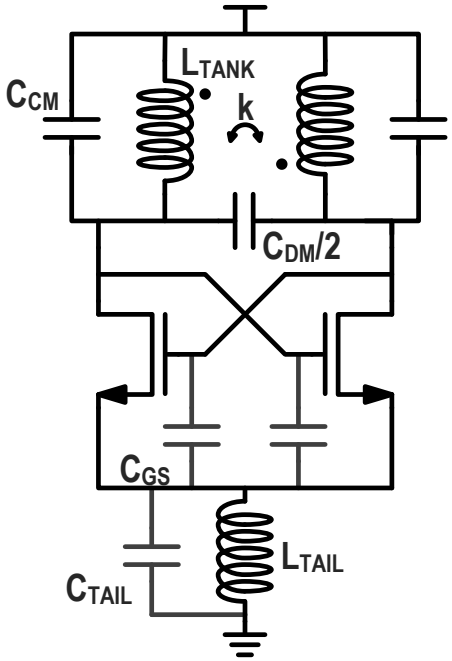
Murphy et. al., *ISSCC 2015.*
M. Shahmohammadi et al., *ISSCC 2015.*

$$F = 1 + \gamma$$

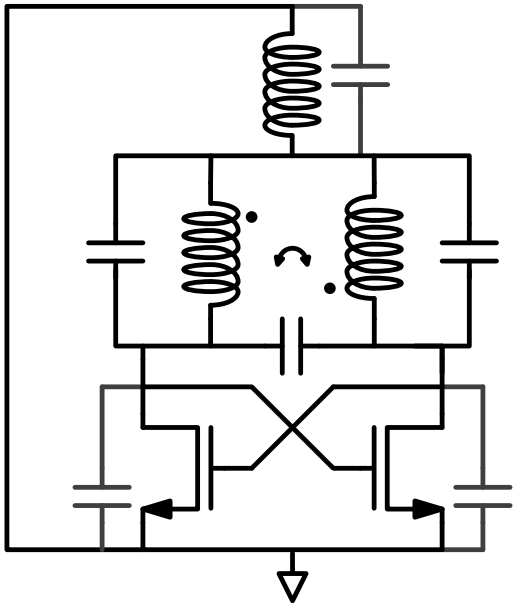
$$\eta \approx 80\%$$

- Within **1dB** of maximum theoretical FOM

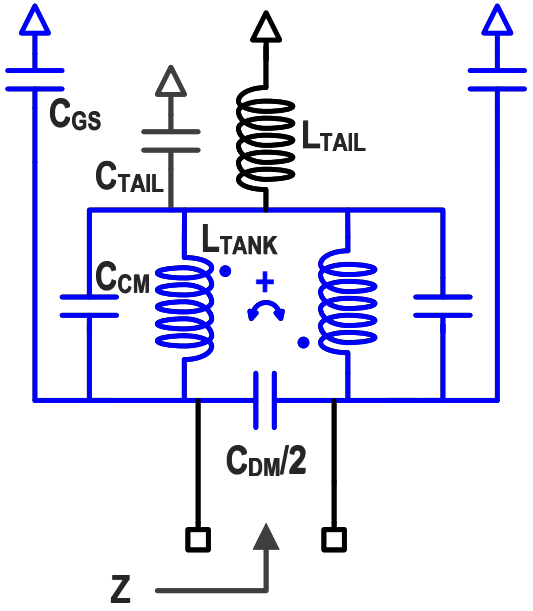
Prior Art: Hegazi's VCO



With DC-Biasing

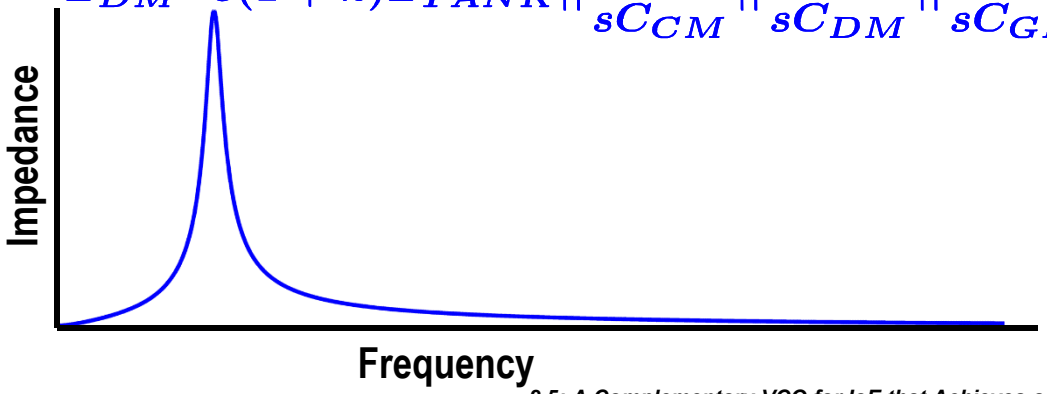


AC-Equivalent

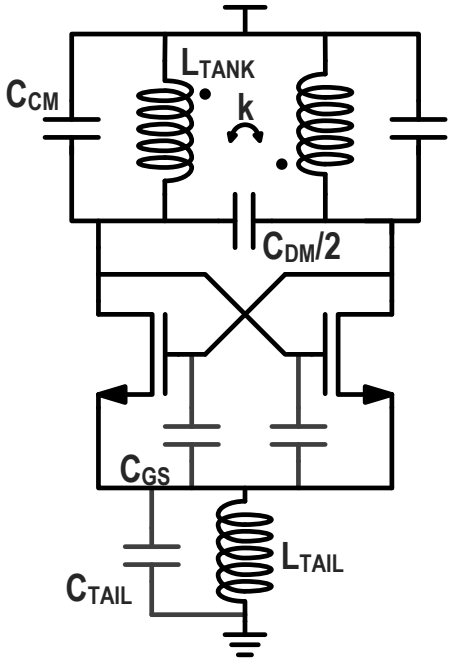


Tank-Impedance

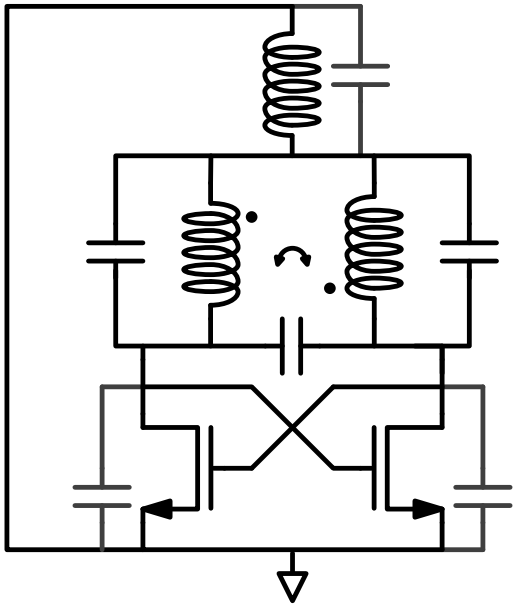
$$Z_{DM}=s(1+k)L_{TANK}||\frac{1}{sC_{CM}}||\frac{1}{sC_{DM}}||\frac{1}{sC_{GD}}$$



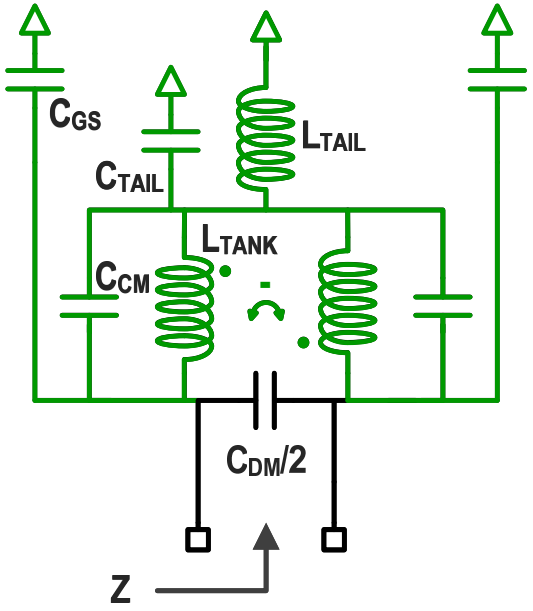
Prior Art: Hegazi's VCO



With DC-Biasing



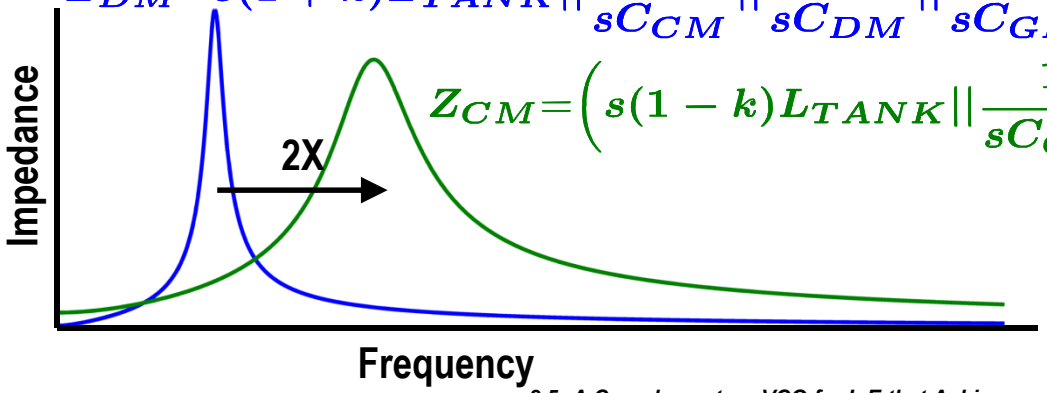
AC-Equivalent



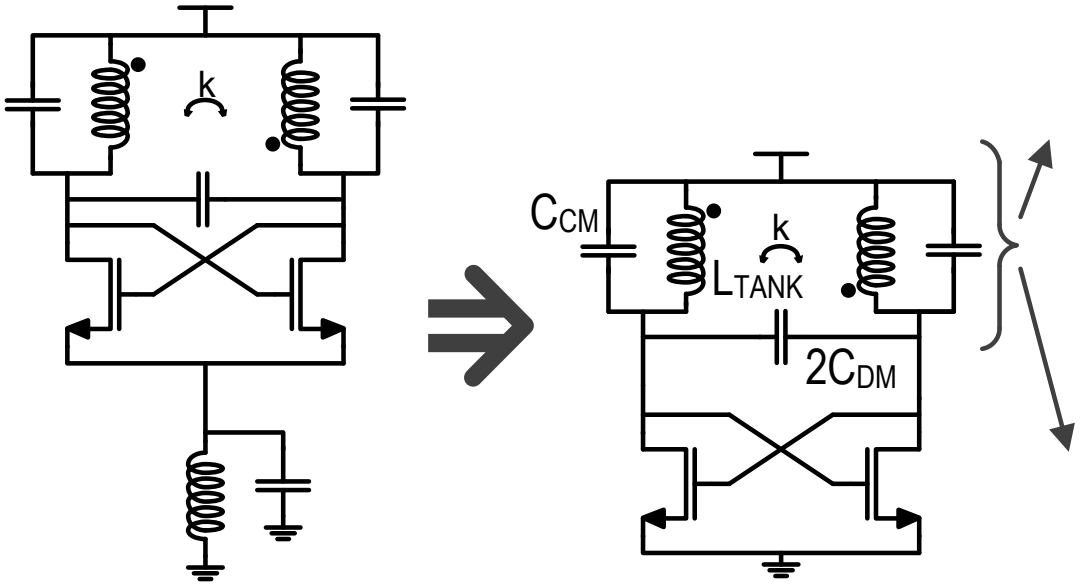
Tank-Impedance

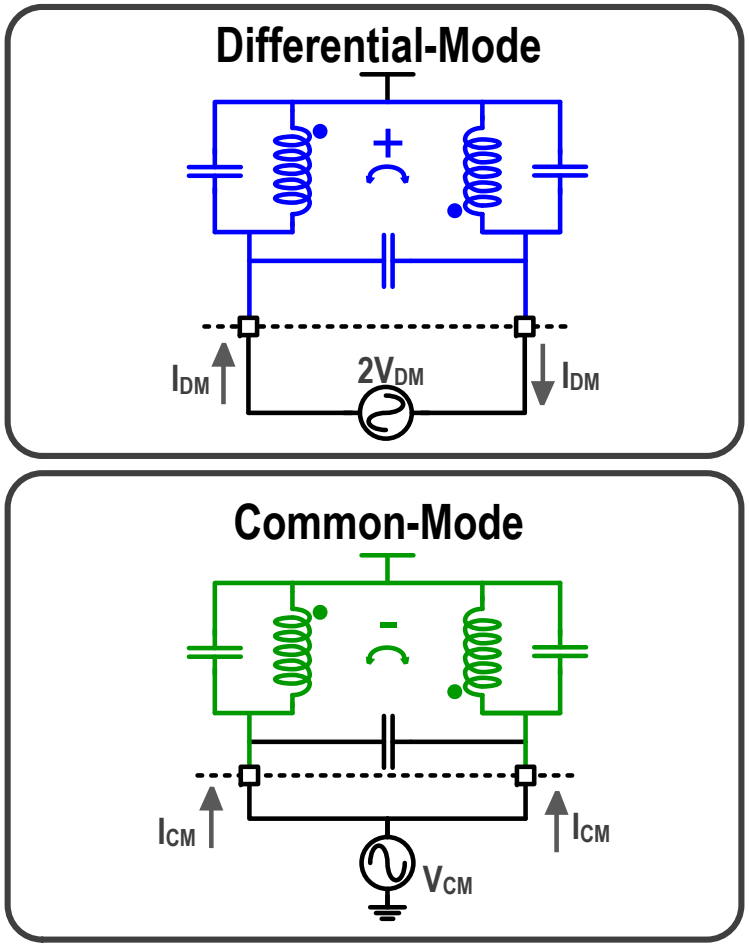
$$Z_{DM}=s(1+k)L_{TANK}||\frac{1}{sC_{CM}}||\frac{1}{sC_{DM}}||\frac{1}{sC_{GD}}$$

$$Z_{CM}=\left(s(1-k)L_{TANK}||\frac{1}{sC_{CM}}+s2L_{TAIL}||\frac{2}{sC_{TAIL}}\right)||\frac{1}{sC_{GD}}$$



Prior Art: Implicit Common-Mode Resonance VCO

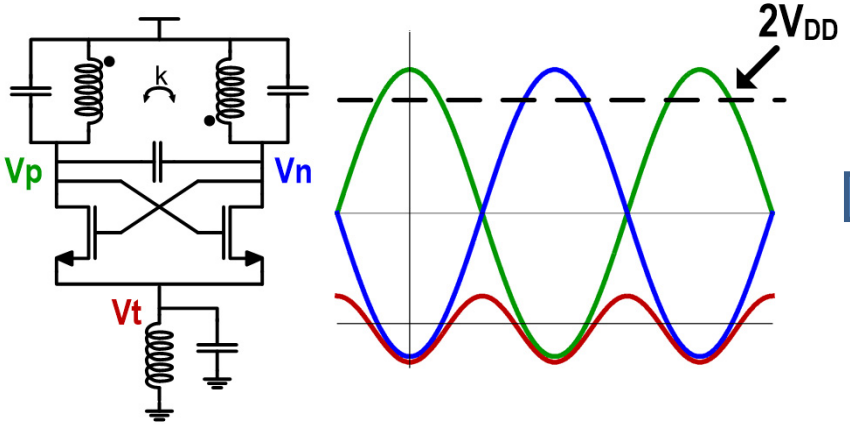




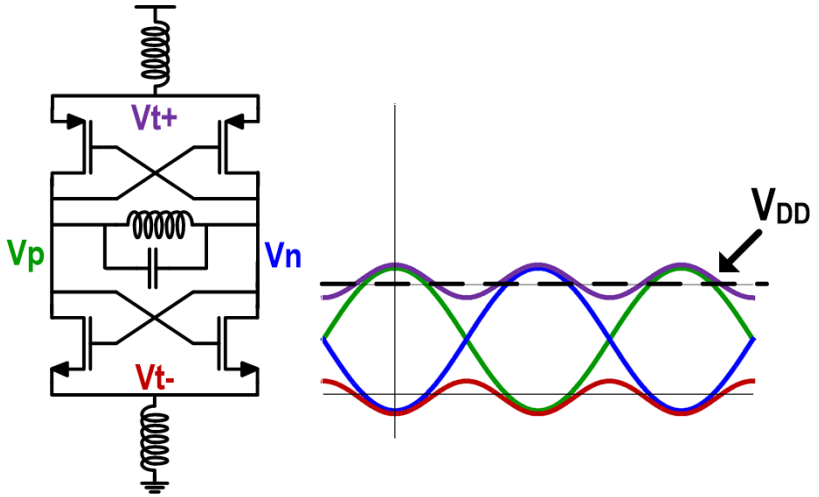
→ No Tail inductor
→ Simplified Layout
→ CM well-defined
→ Fully CMOS Equivalent?

Murphy et. al., *ISSCC 2015.*
M. Shahmohammadi et al., *ISSCC 2015.*

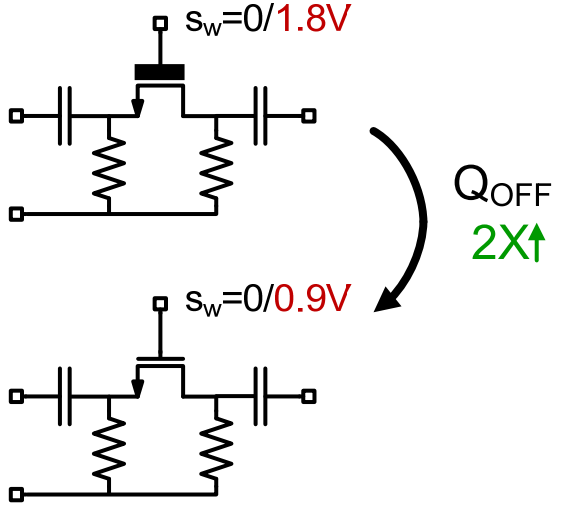
NMOS versus CMOS

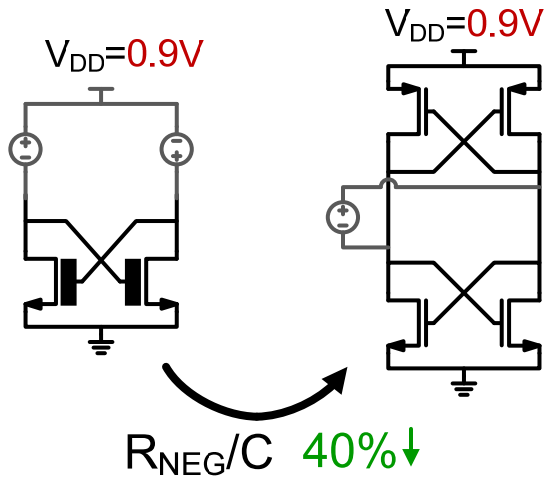


Hegazi – NMOS
(Thick Oxide I/O Devices ☹)

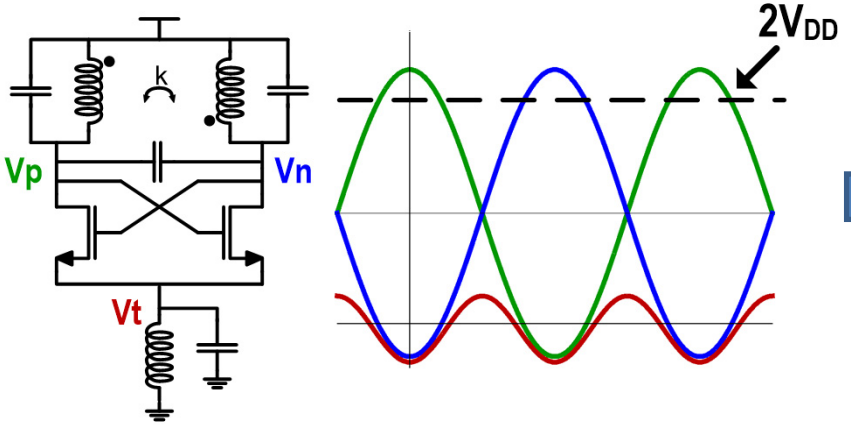


Hegazi – CMOS
(Thin Oxide Core Devices ☺)

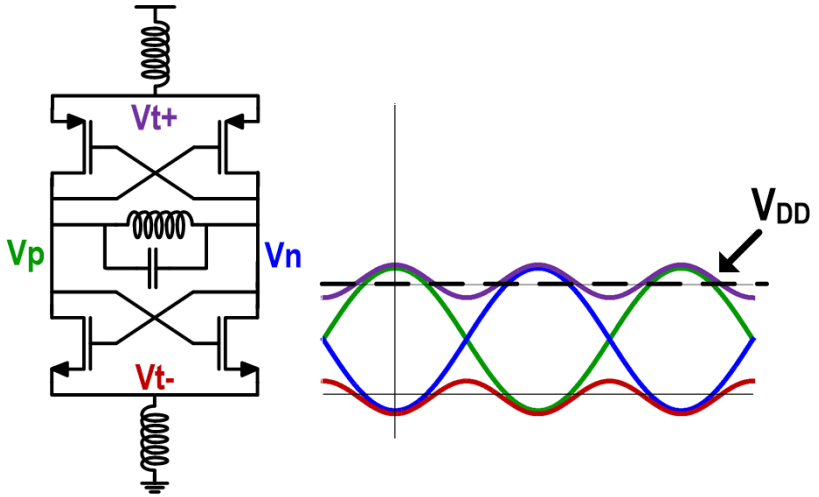




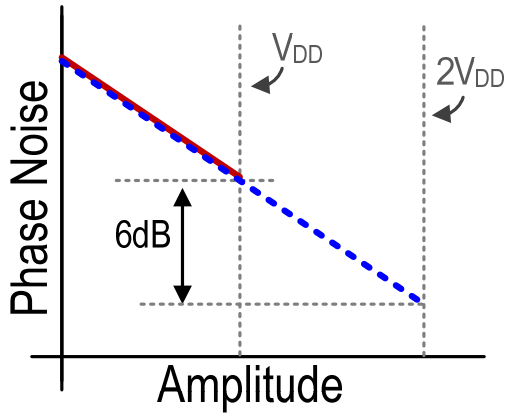
NMOS versus CMOS

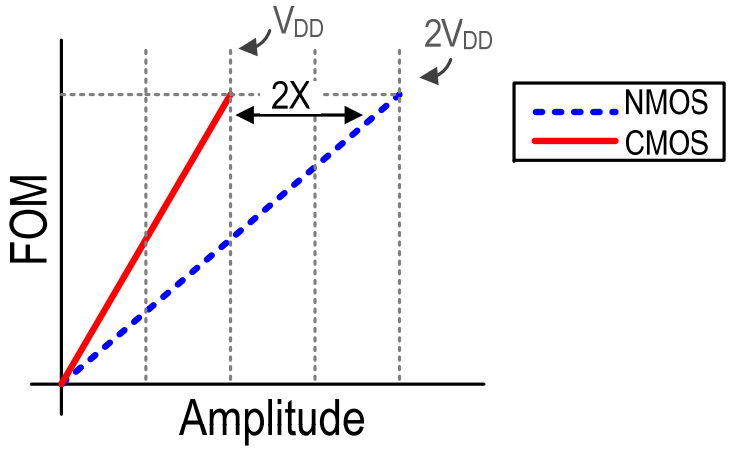


Hegazi – NMOS
(Thick Oxide I/O Devices ☹)



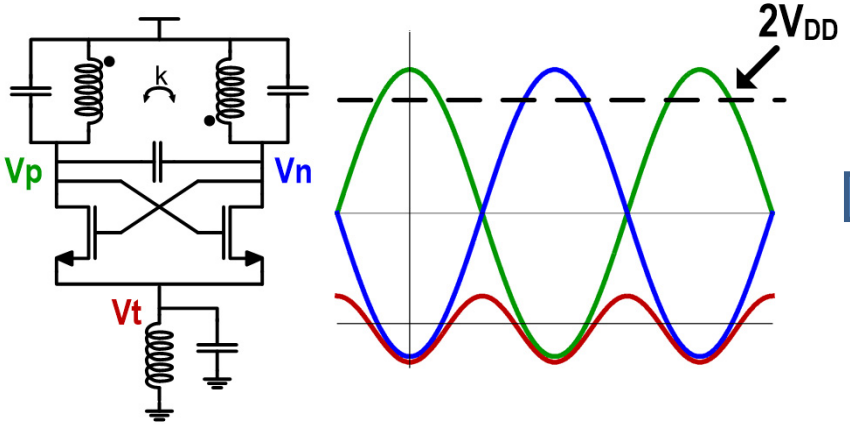
Hegazi – CMOS
(Thin Oxide Core Devices ☺)



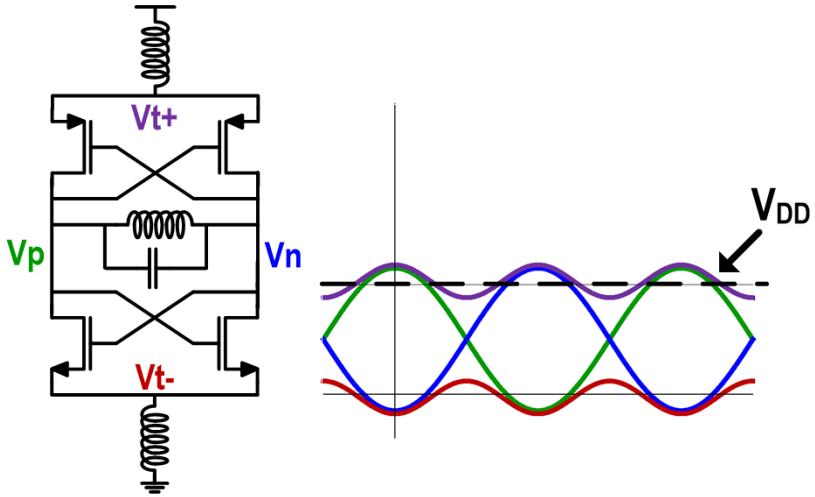


CMOS more suitable for low power design…

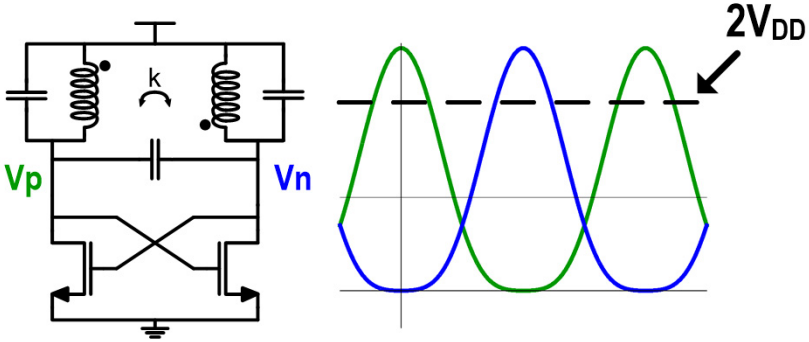
NMOS versus CMOS



Hegazi – NMOS
(Thick Oxide I/O Devices ☹)



Hegazi – CMOS
(Thin Oxide Core Devices ☺)

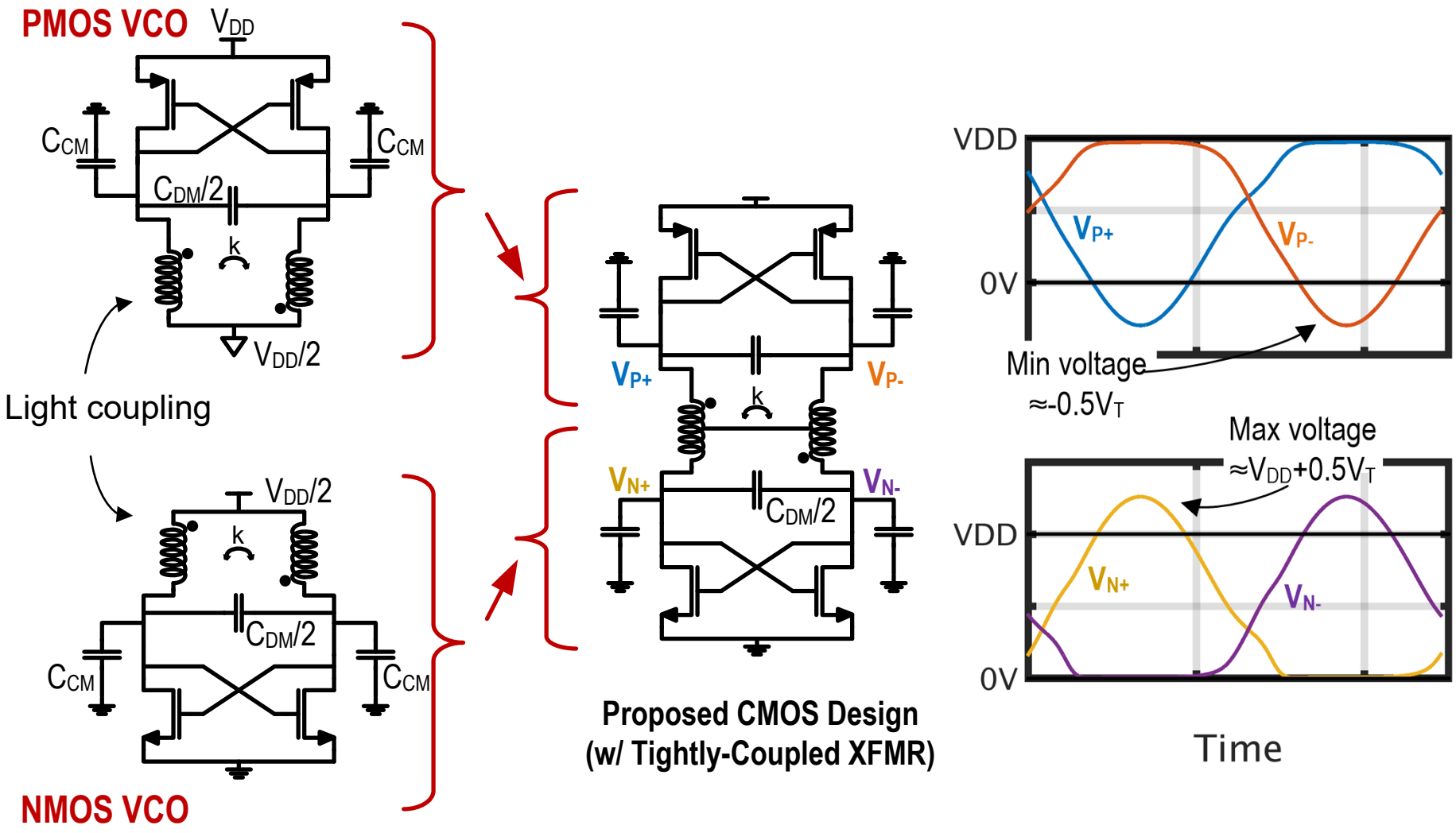


Implicit – NMOS
(Thick Oxide Devices ☹)

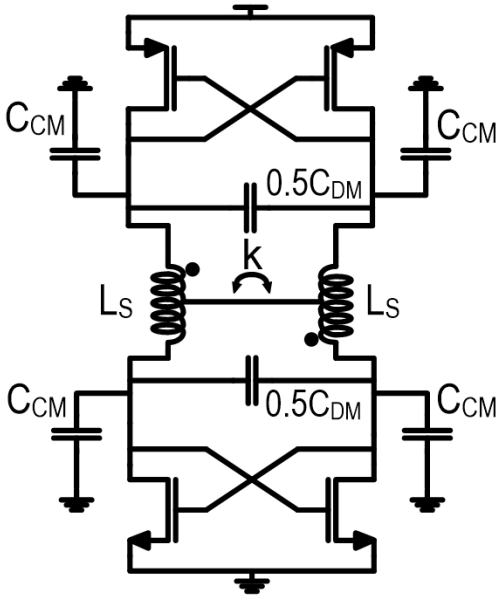
?

Implicit – CMOS
(Suitable for Low-Power Design)

Proposed CMOS Equivalent

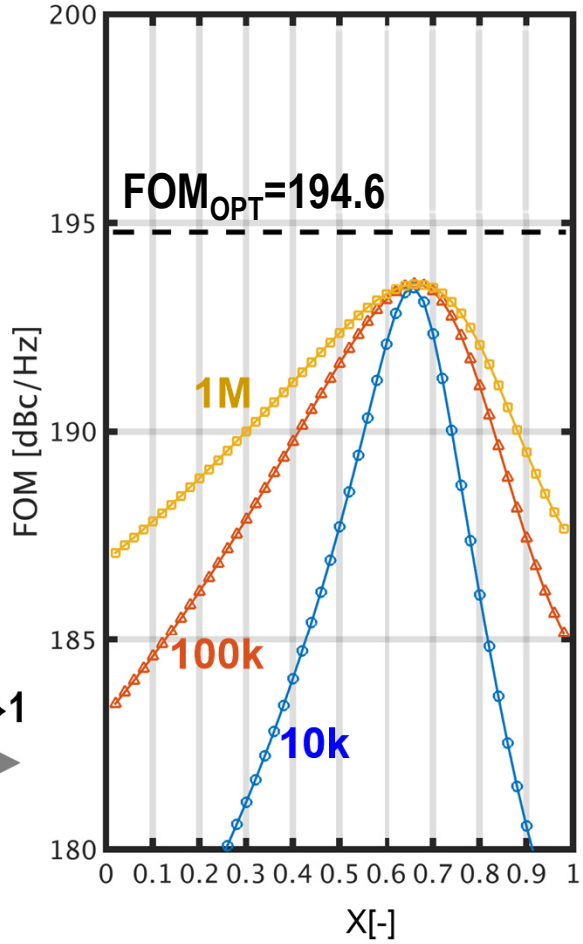


Idealized Simulation



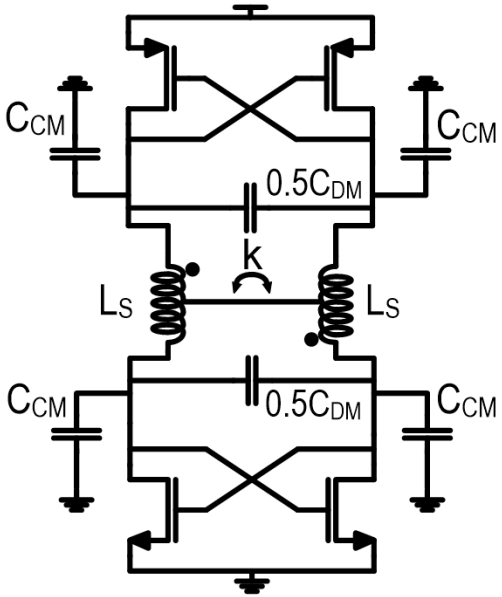
k=0.2
Q = 10
L_S= 666pH
C_{CM}= (1-X)C_P
C_{DM}= XC_P
f_0=2GHz

X= 0⟶1



$$FOM\{\Delta\omega\} = \frac{\left(\frac{\omega_0}{\Delta\omega}\right)^2}{\mathcal{L}\{\Delta\omega\}P_{DC[mW]}} = Q^2\frac{\eta}{F}\frac{2}{kT}1\text{m}$$

Idealized Simulation



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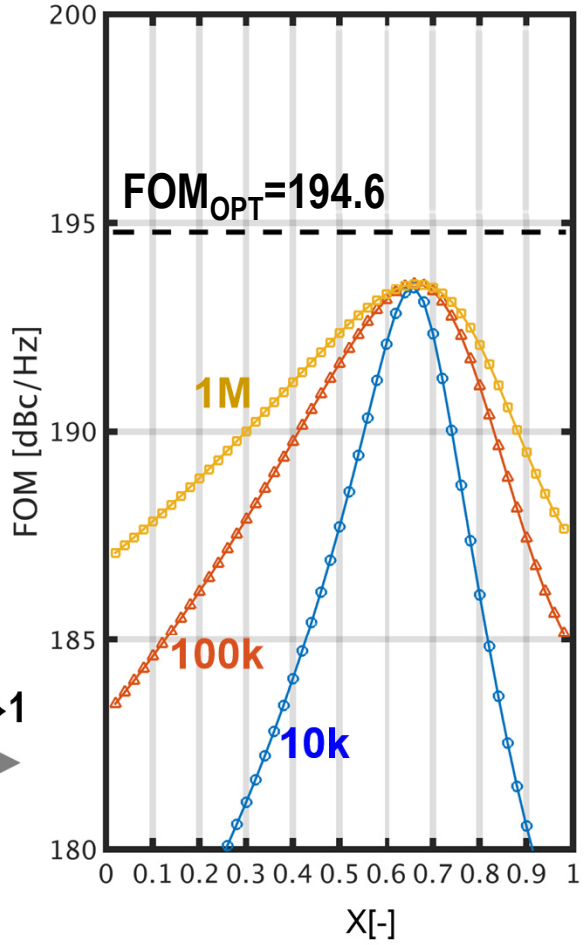

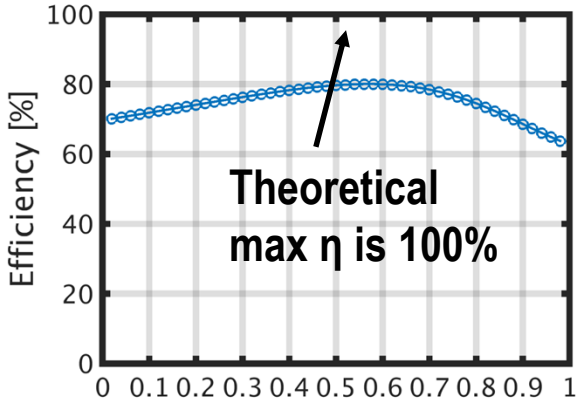

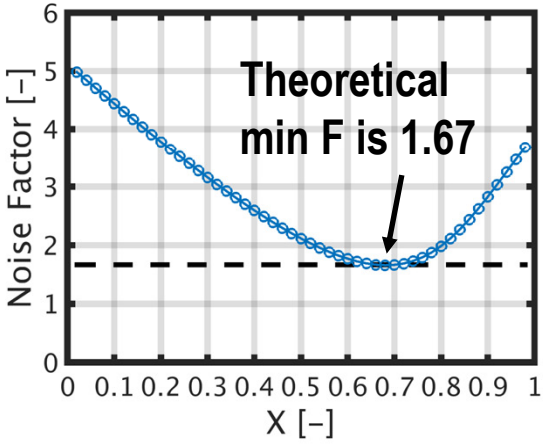

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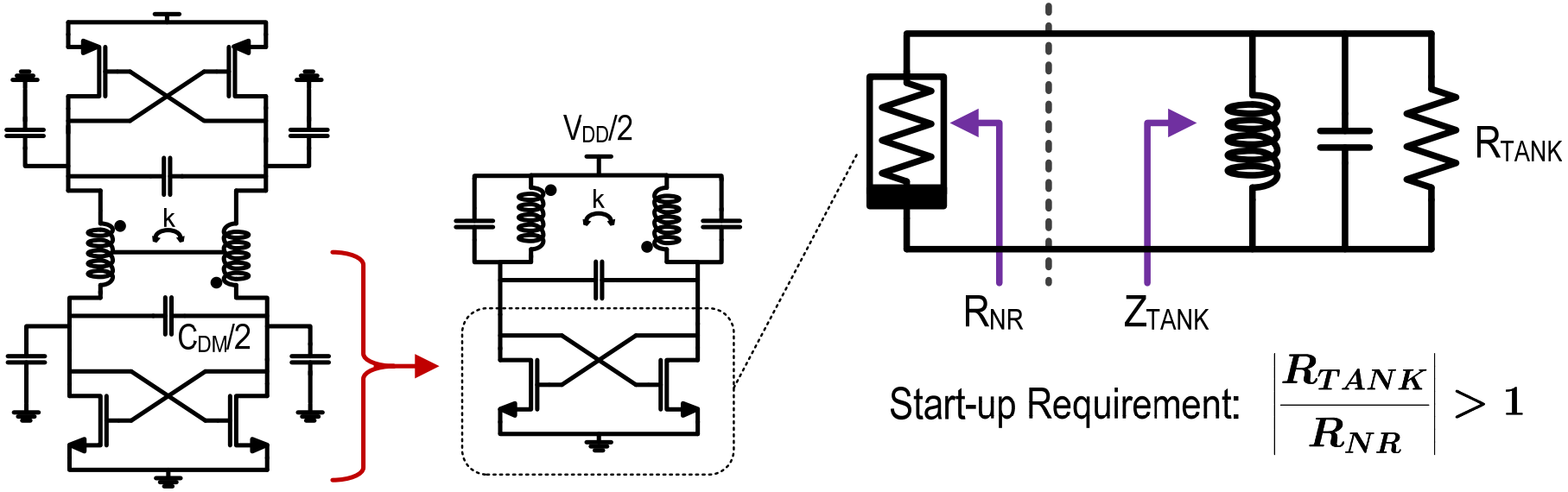
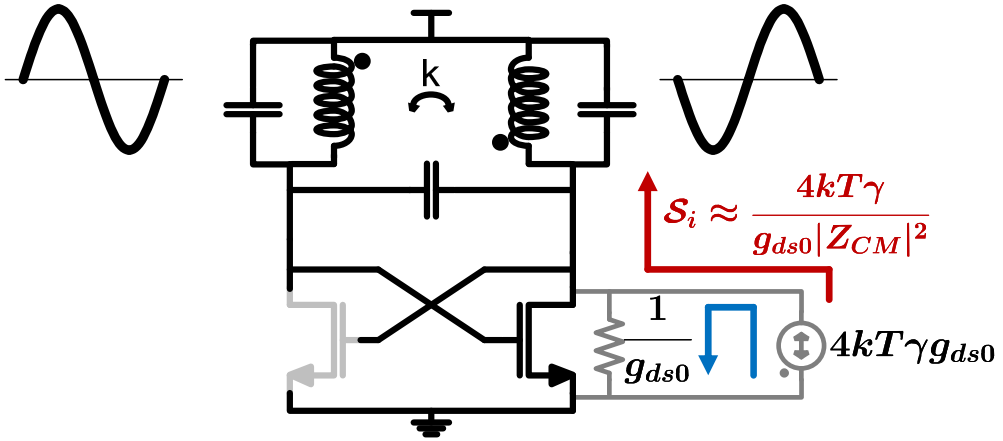
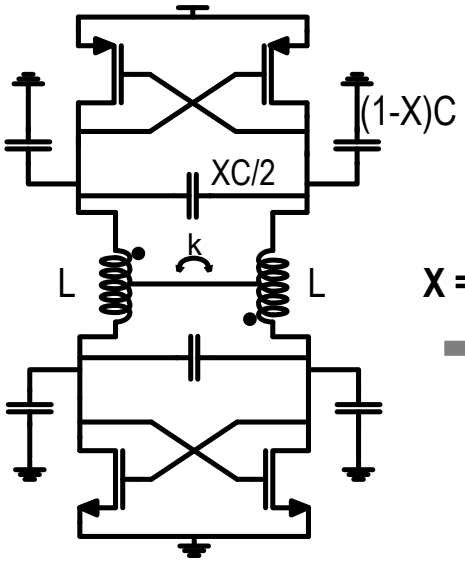
Loop Gain Sensitivity (1/2)



- Large Differential Pair
  - Hard switching
  - Lower noise injection
  - Lower flicker noise

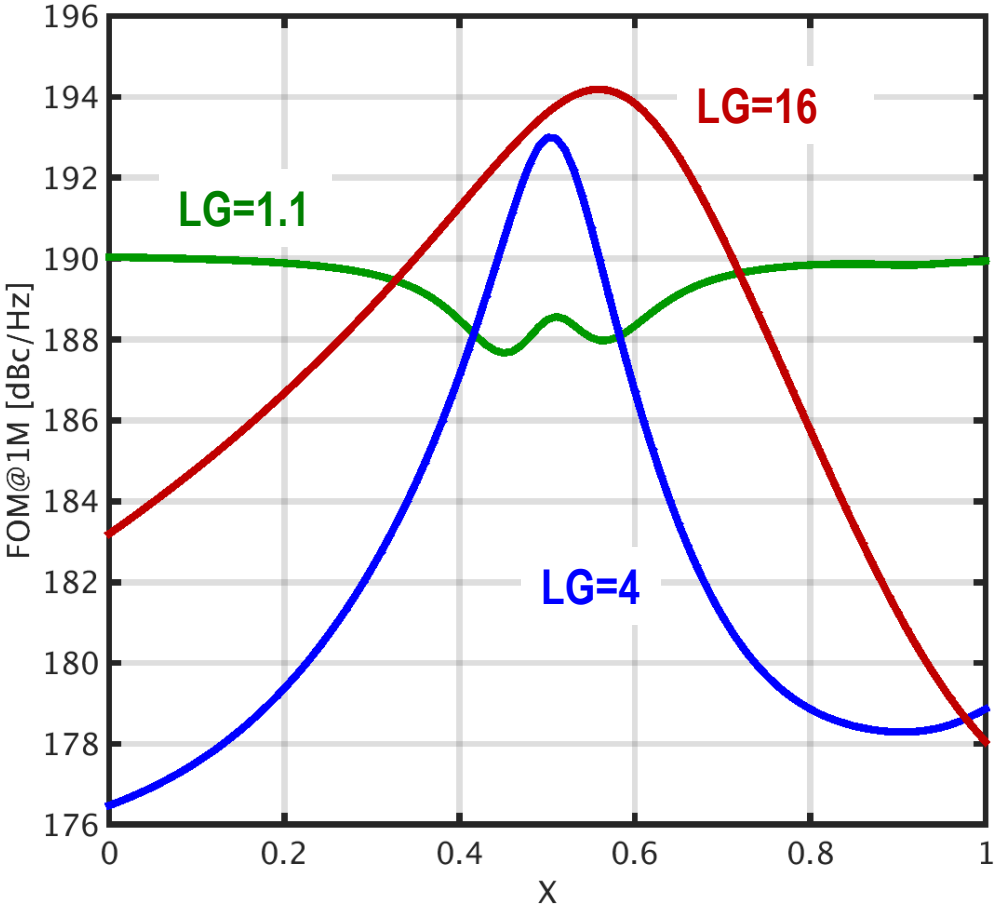


Loop Gain Sensitivity (2/2)



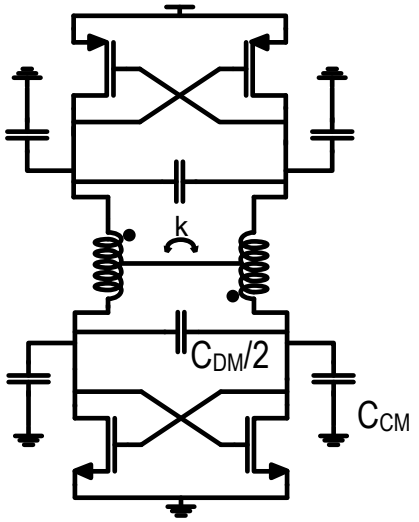
X =0→1

Q = 10
k = 0.33
f_0=3.7GHz



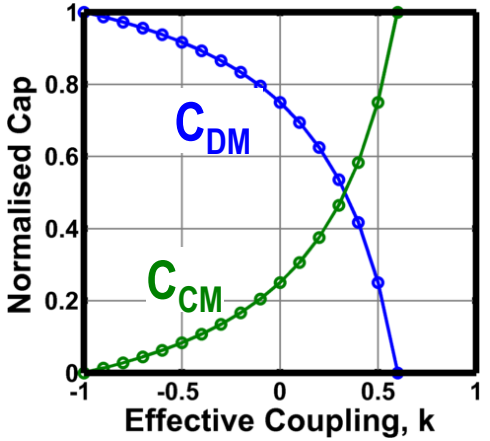
- Increasing loop gain reduces CM tuning sensitivity
- Prototype employs loop gain ≈ 5

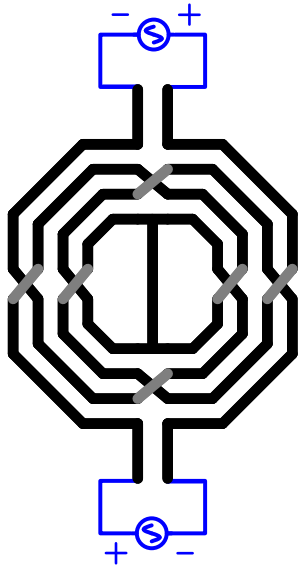
XFMR Design

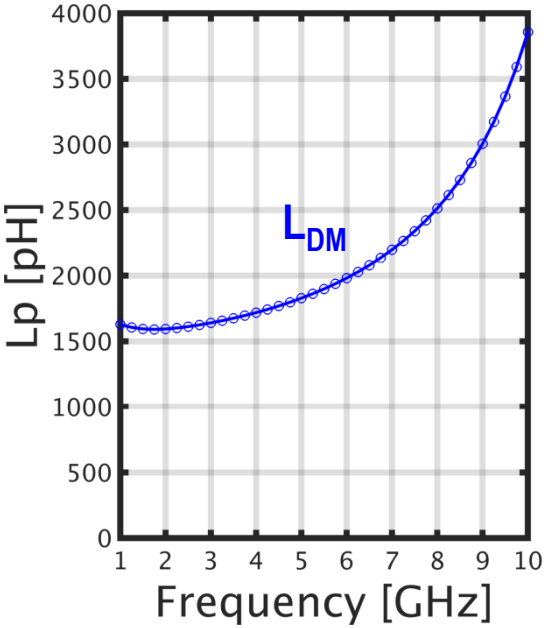


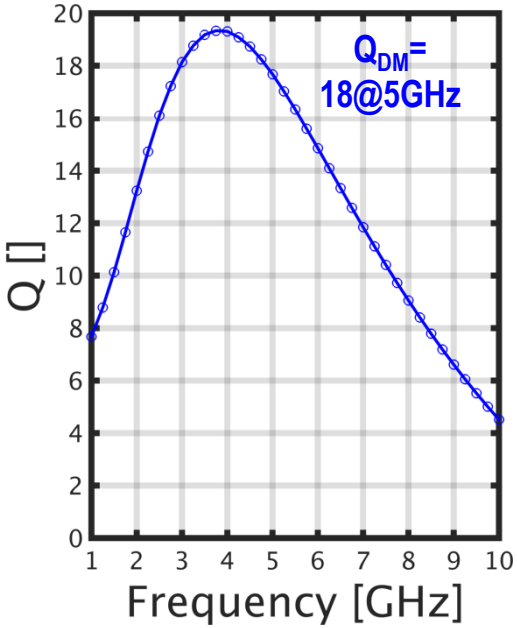
Optimal Performance Condition

$$\frac{C_{DM}}{C_{CM}} = \frac{3-5k}{1+k}$$

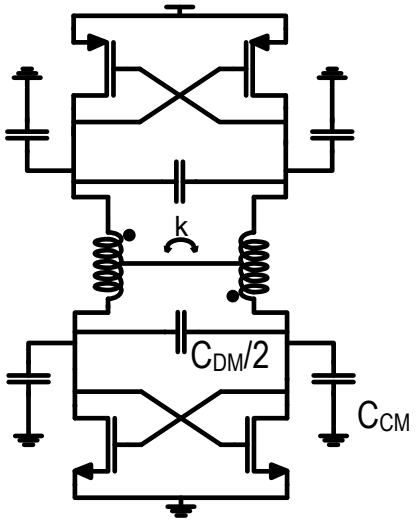








XFMR Design



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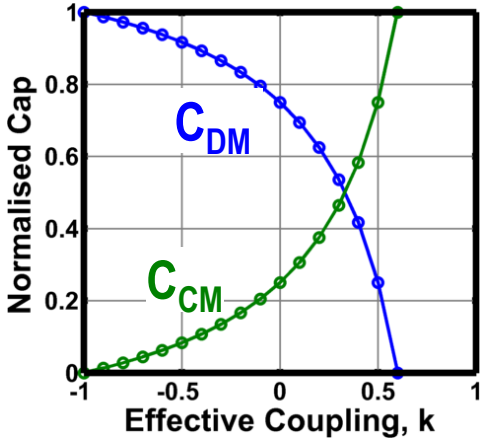
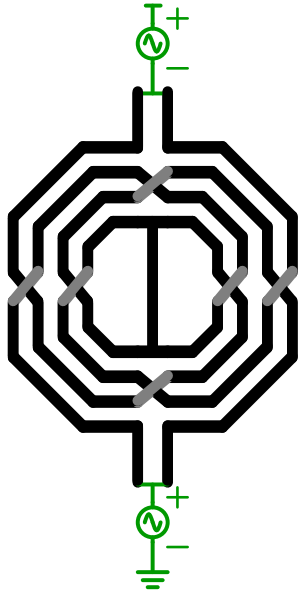
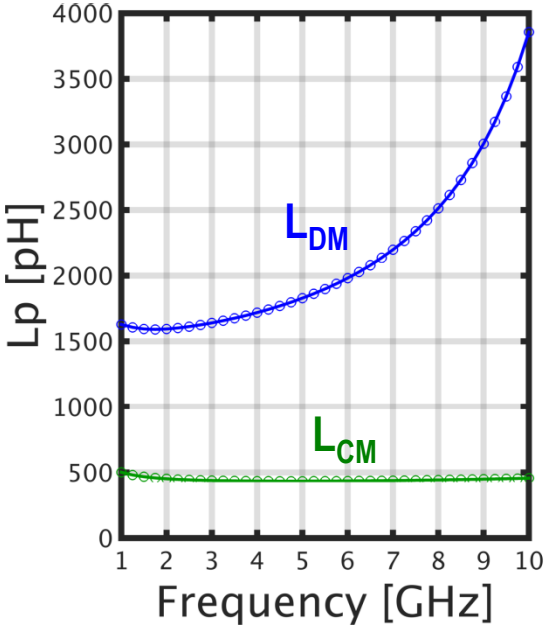
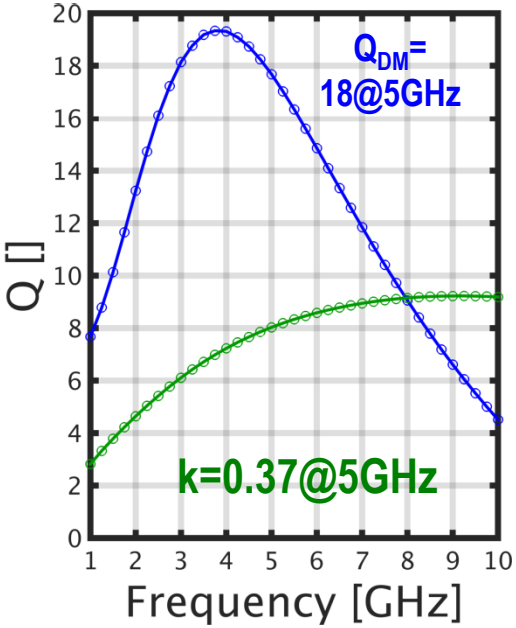


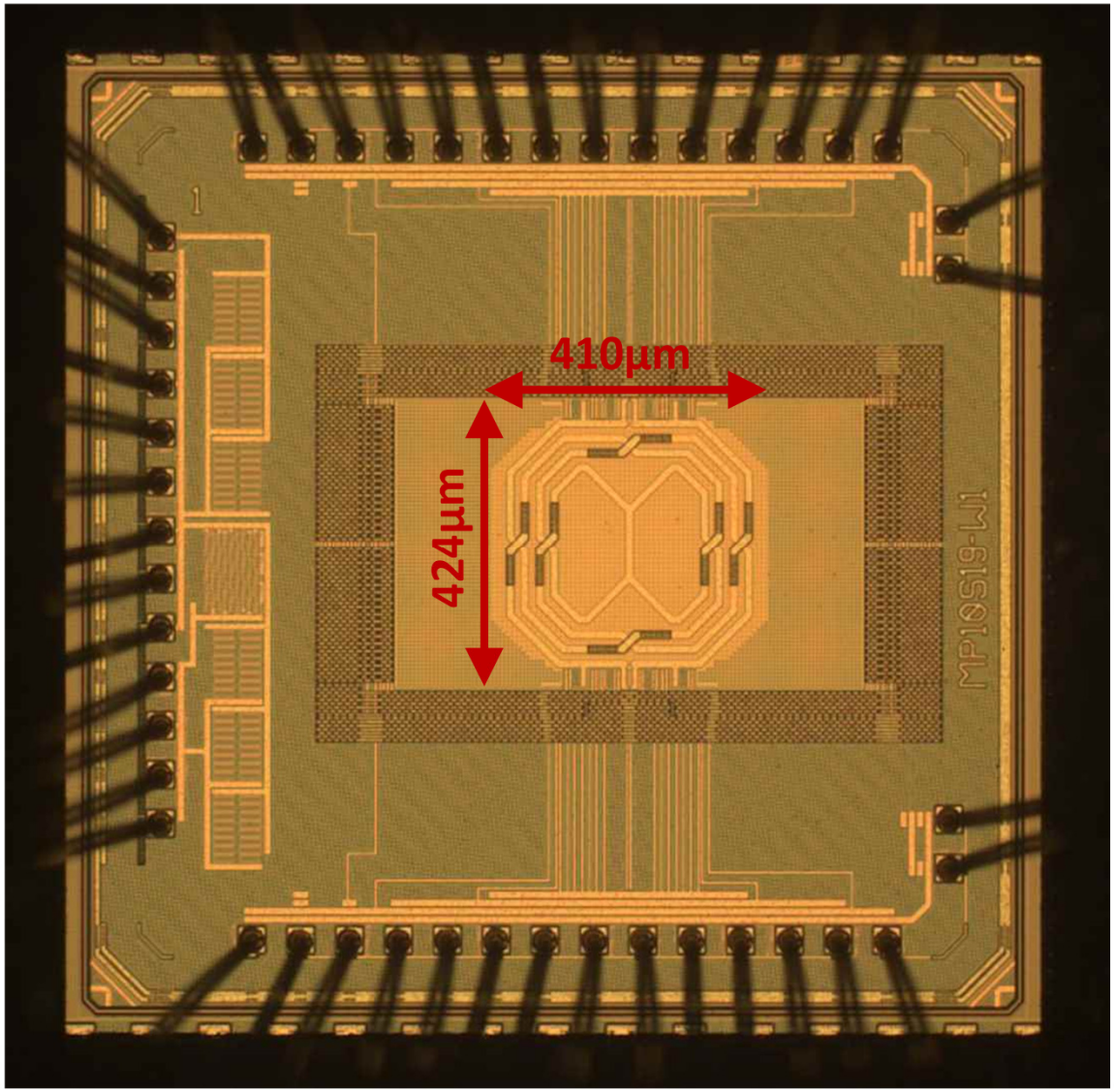






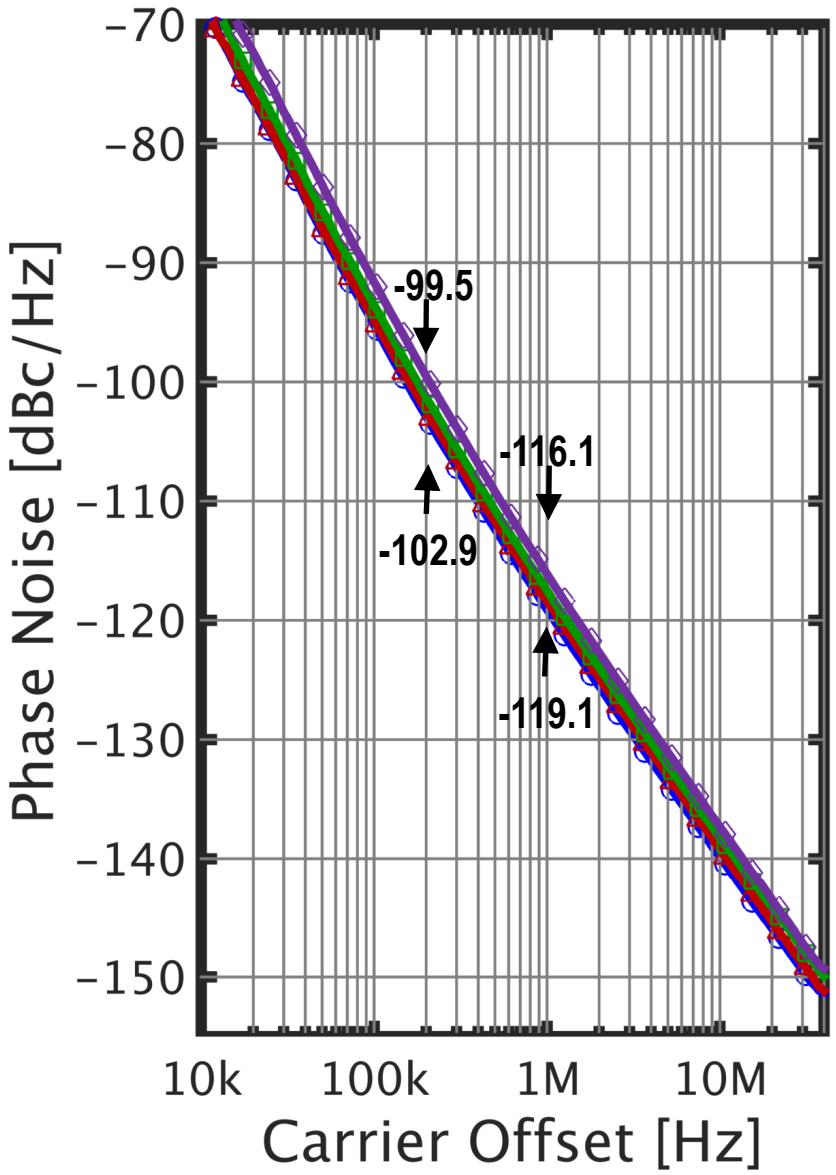
QCM= 9@10GHz

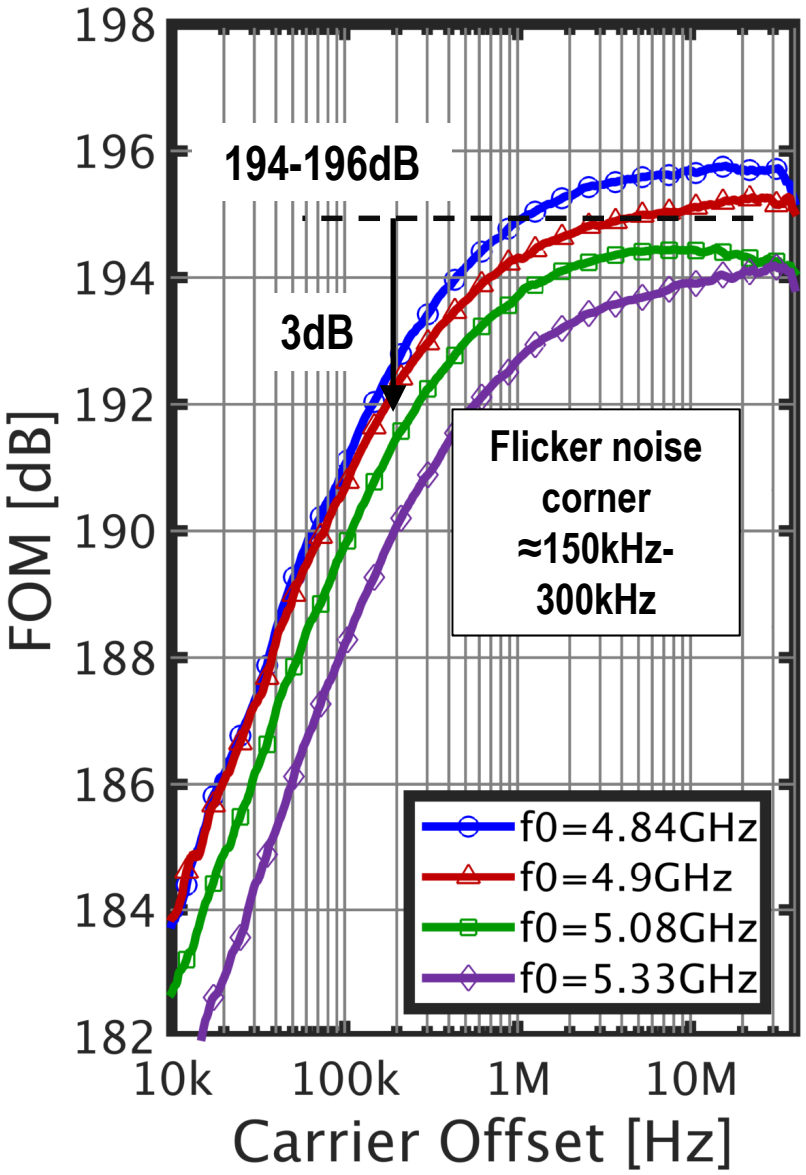
Die Photo



28nm Technology (Only minimum length thin-oxide devices used)

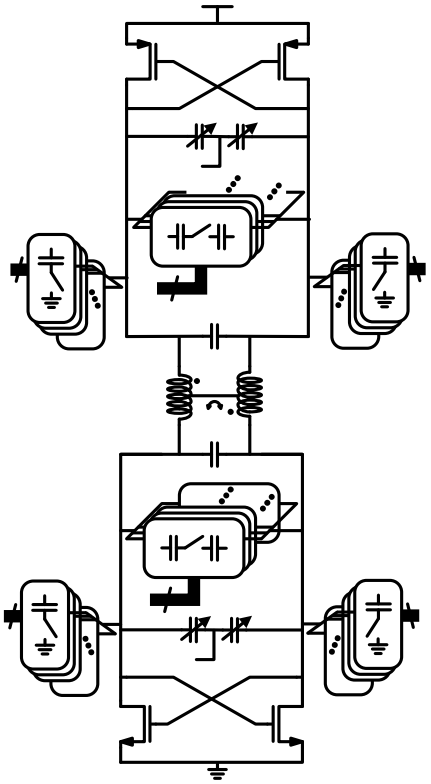
Measurement Results: Phase Noise & FOM

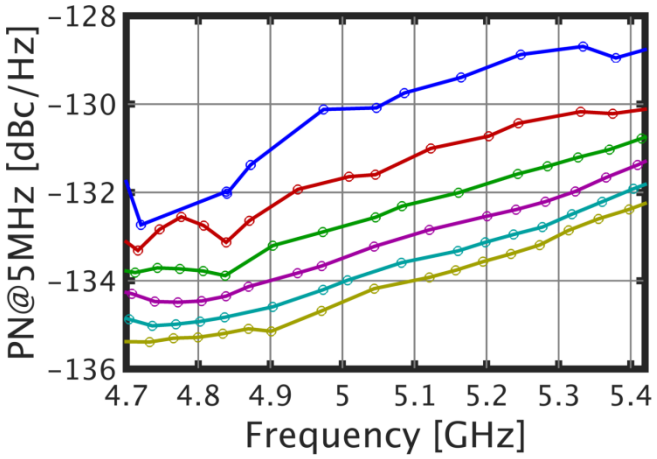


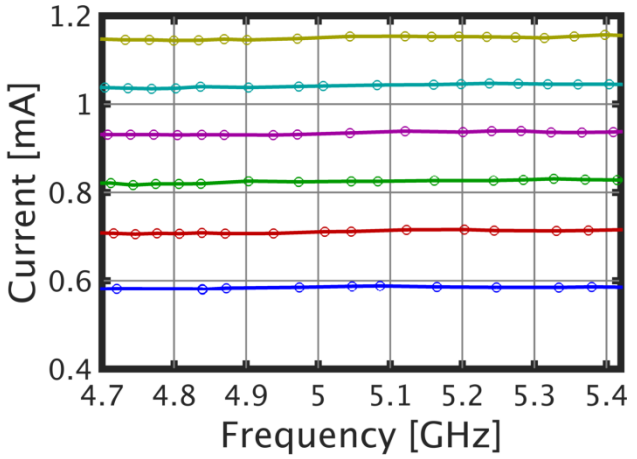


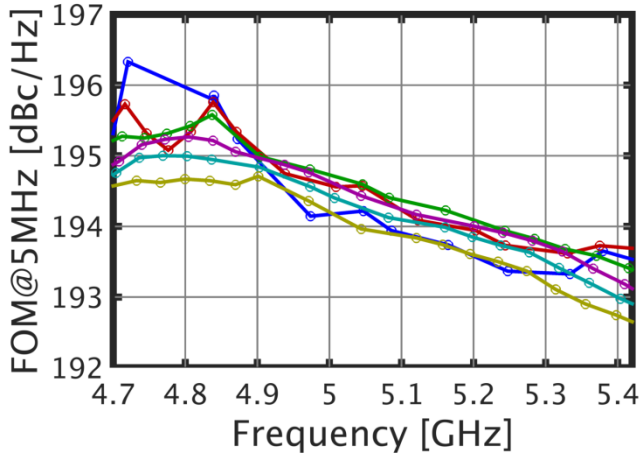
Measurement Results: versus Supply

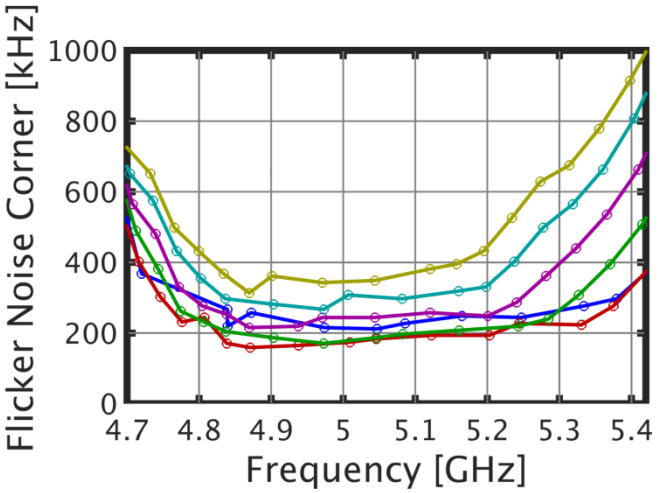
V_{DD}=0.65V→0.9V







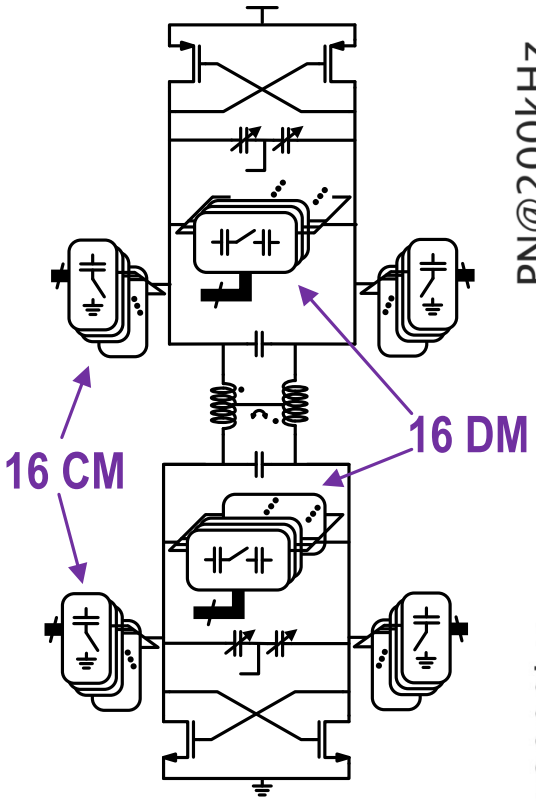


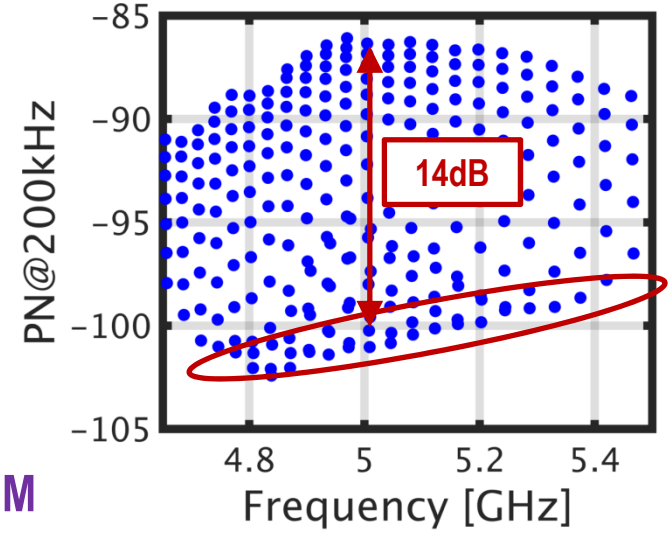


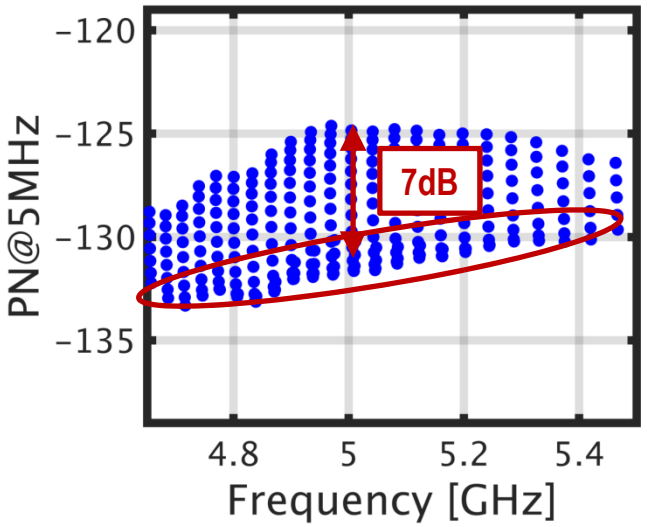
- Voltage controlled design
- Low threshold devices used... lower supply better

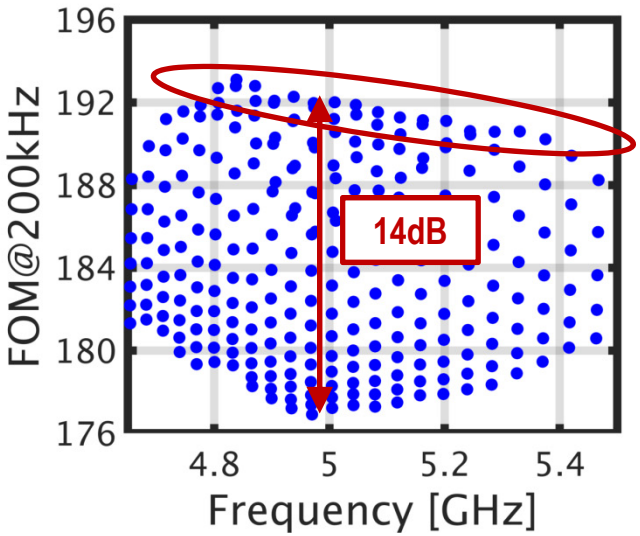
VDD=0.65
VDD=0.7
VDD=0.75
VDD=0.8
VDD=0.85
VDD=0.9

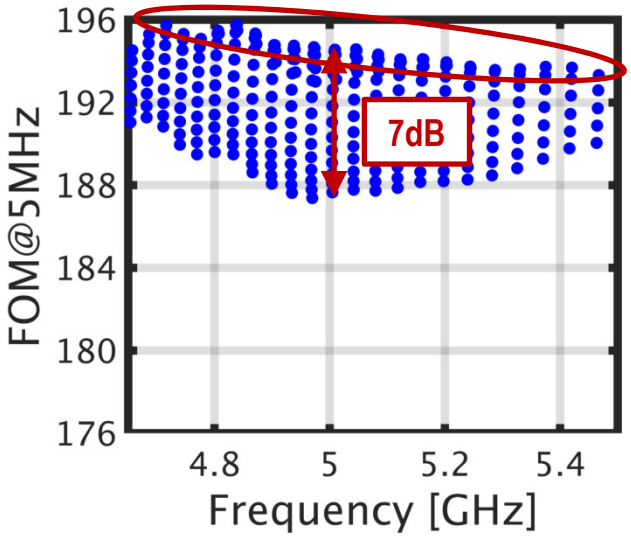
Measurement Results: Importance of Common-Mode Tuning











- 289 digital tuning codes
- Common-mode resonance improves FOM by up to 14dB@200kHz

Table of Comparison with Published VCOs

	JSSC 2001 (Hegazi)	JSSC 2015 (Garampazzi)	This Work
Topology	NMOS $2F_{LO}$ Tail Tuning	CMOS $2F_{LO}$ Tail Tuning	CMOS $2F_{LO}$ Implicit Resonance
Technology	0.35µm	55nm	28nm
Supply Voltage	2.5	1.5	0.7
Frequency Range [GHz]	1-1.2 (18%)	7.4-8.4 (13%)	4.7-5.4 (13.8%)
Phase Noise [dBc/Hz @ 3MHz]	-153.2	-133	-126.9
Power [mW]	9.1	6.3	0.5
FOM [dB] (Thermal Region)	195	194.3-195.6	**194-196**
FOM [dB] (@100kHz)	185*	185*	**188-191**
Core Area [mm^2]	N/A	0.19	0.18
Passives	2 Inductors	1 Inductor 1 XFMR	1 XFMR

*Estimated from plots

Conclusions

- A CMOS VCO topology with implicit common-mode resonance
  - Uses a single transformer
  - Suitable for low power applications
  - Within 1dB of theoretically achievable FOM
  - Nulls flicker noise

- Fabricated prototype
  - High FOM (≈194-196)
  - Low flicker noise corner (≈150kHz-300kHz)

A 190.5 GHz Mode-Switching VCO with 20.7% Continuous Tuning Range and Maximum Power of -2.1dBm in 0.13µm BiCMOS

Rouzbeh Kananizadeh and Omeed Momeni

High-Speed Integrated Electronic Systems Lab (HISIES)

University of California, Davis, Ca

Outline

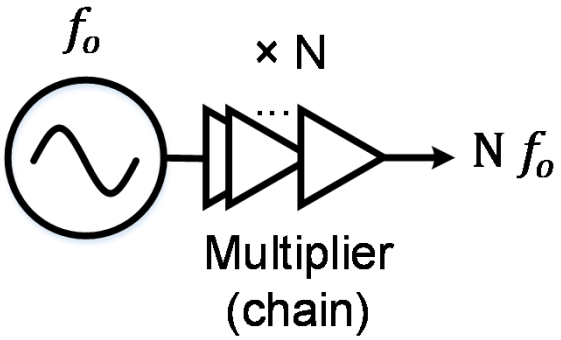
- **Motivation**
- Mode-switching VCO Circuit Architecture
- Modes of operation of the VCO
- Measurement Results
- Conclusion

Motivation

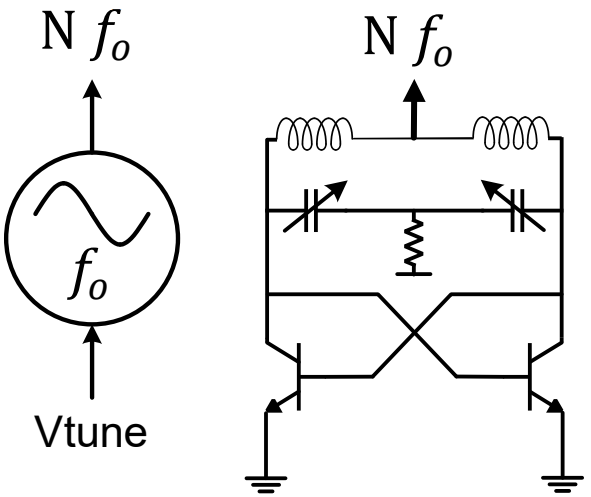
- Applications for wideband signal generation at mm-wave and THz frequencies include
  - Spectroscopy
    - Wideband signals for signature detection of materials
  - High data-rate communication
    - Data-rate is a direct function of bandwidth
  - High resolution radar
    - Range resolution is a function of bandwidth
    - Azimuth resolution is a function of frequency
- Demand wideband and powerful Signal sources

mm-wave and THz Signal Sources

- Frequency Multiplier/amplifier chain
  - Wider bandwidth
  - High conversion loss
  - More power consumption
  - Larger chip area



- Harmonic VCOs
  - Lower tuning range
  - Less power consumption
  - Smaller chip area



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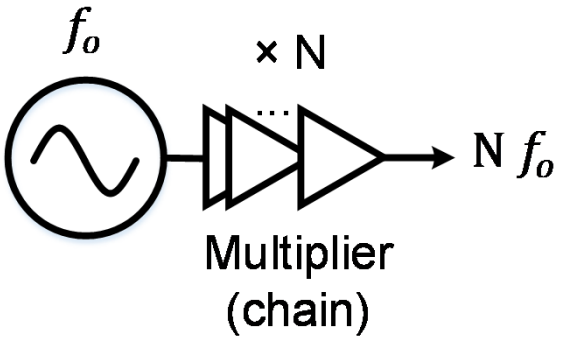

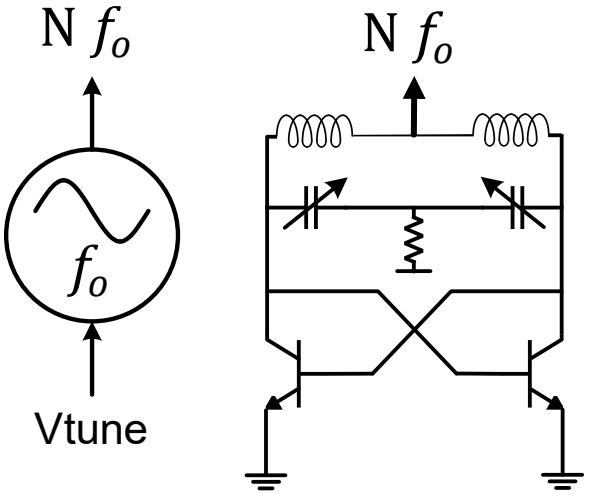

mm-wave and THz Signal Sources

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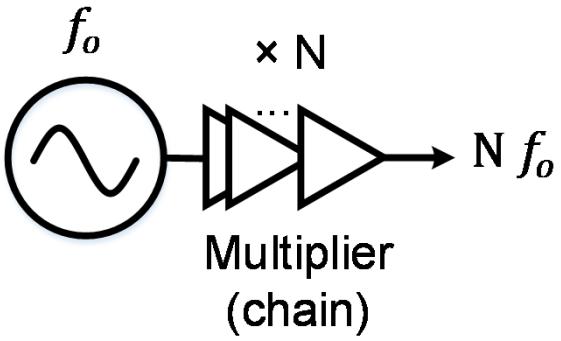
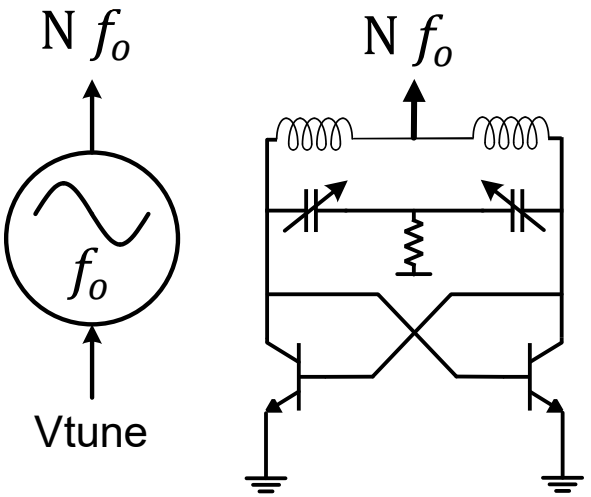


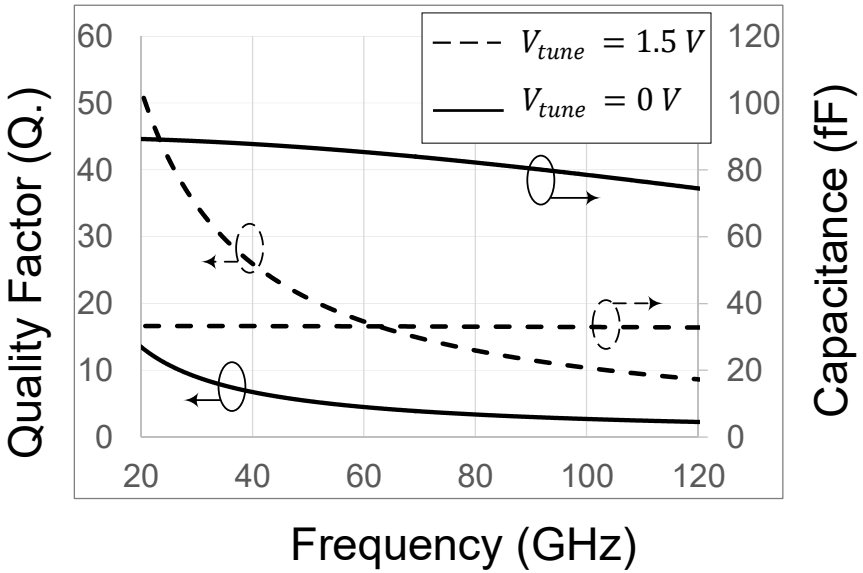
✓ **Harmonic VCOs**
  - Lower tuning range
  - Less power consumption
  - Smaller chip area

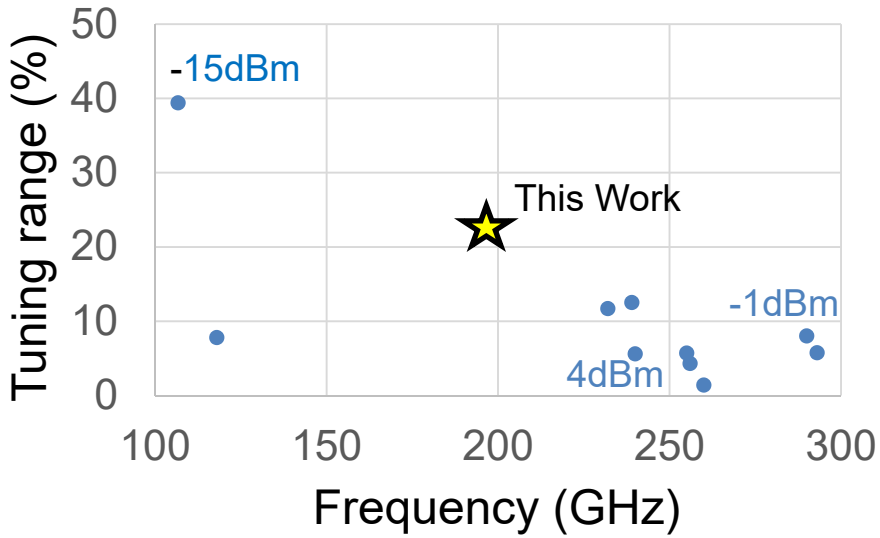


The proposed circuit has significantly improved the tuning range

Challenges of Tuning Range at mm-wave and THZ Frequencies

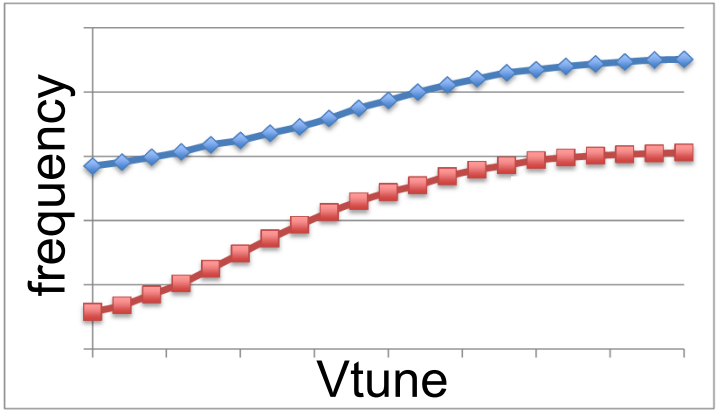
- Low quality factor of varactors
  - Impedes Oscillation start up
  - Lower oscillation swing
  - Lower harmonic power
- Parasitic capacitance of transistors
  - Comparable to varactors
  - Limits the tuning range

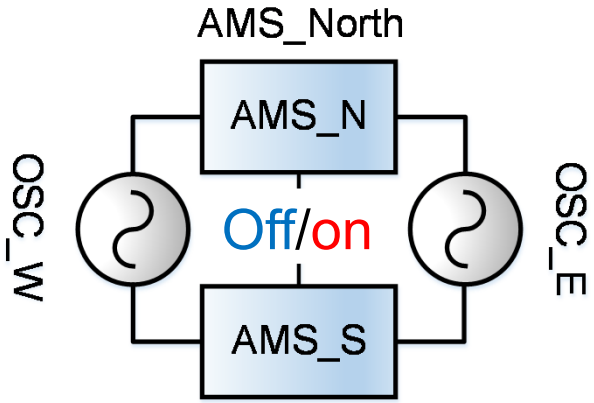




Proposed Approach

- A novel **Active Mode Switching (AMS)** block is used to couple two identical VCOs
  - Each mode has separate center frequency
  - Tuning in each mode
  - Overlap between the two modes
- Low-loss mode-switching
  - Strong oscillation for high output power
- Low-Cap. mode-switching
  - High-frequency of operation
  - Wide tuning range

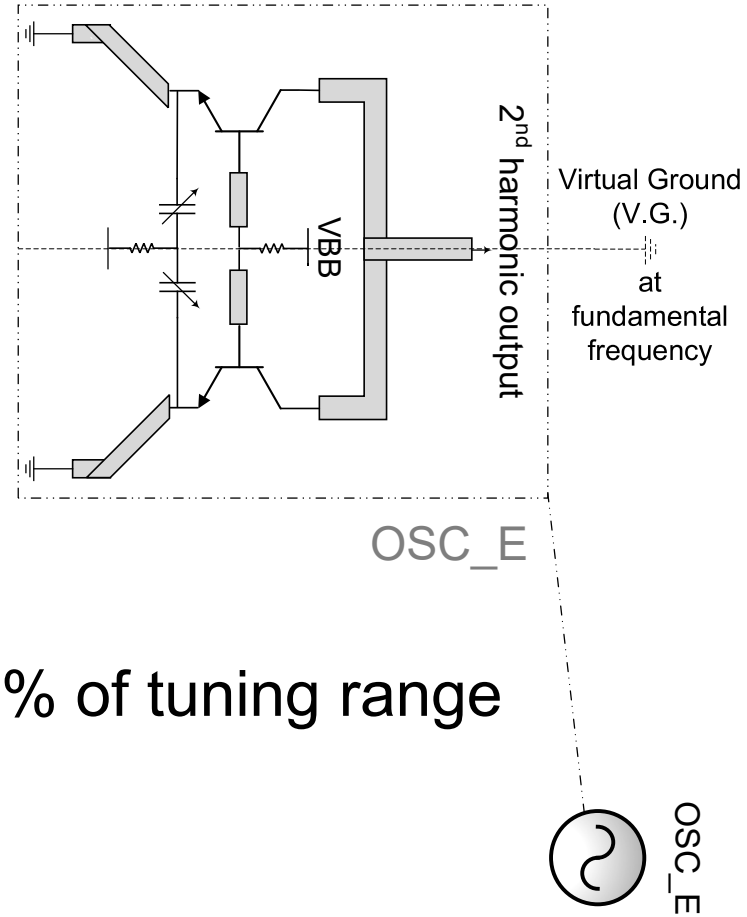




Outline

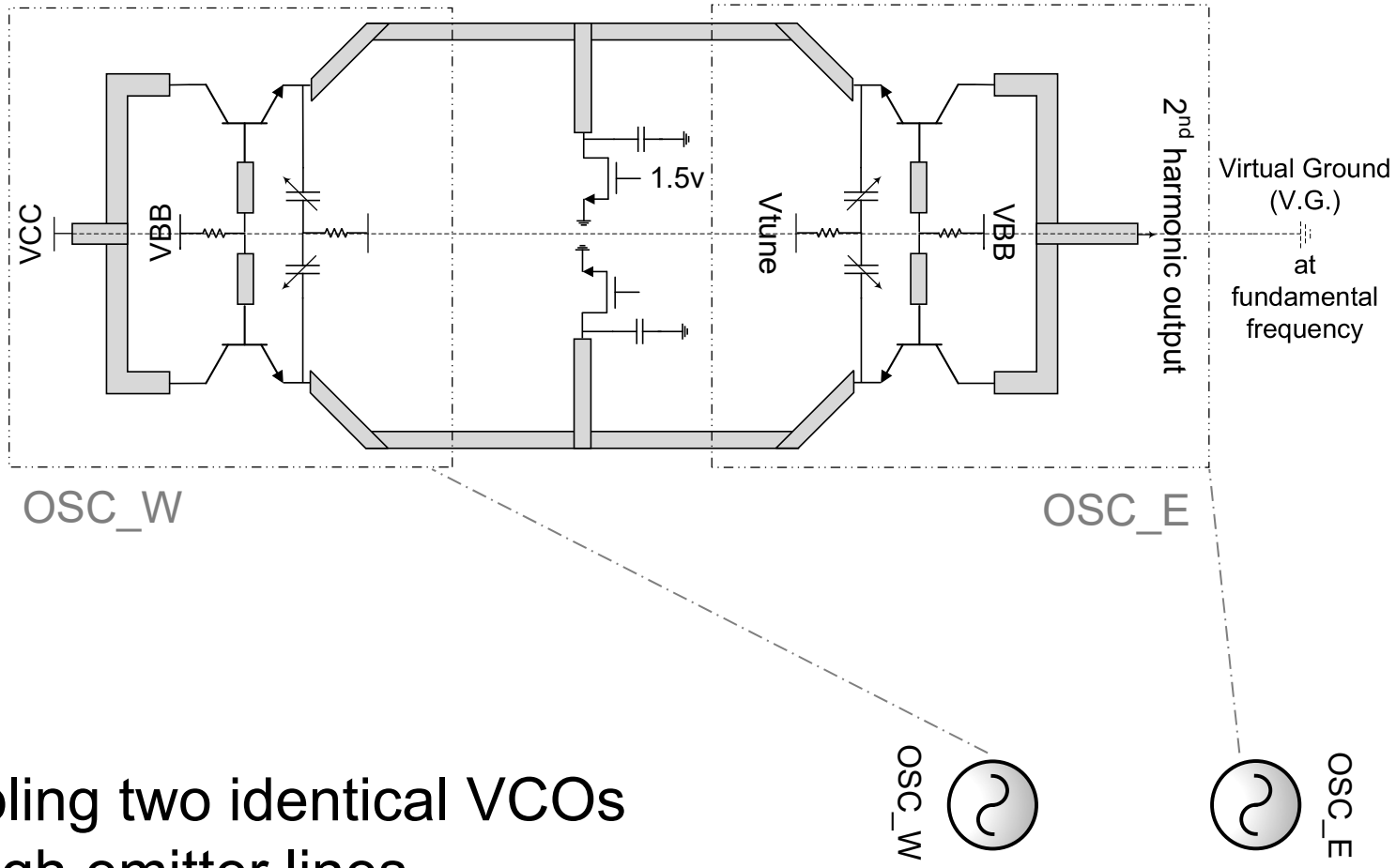
- Motivation
- **Mode-switching VCO Circuit Architecture**
- Modes of operation of the VCO
- Measurement Results
- Conclusion

Core VCO



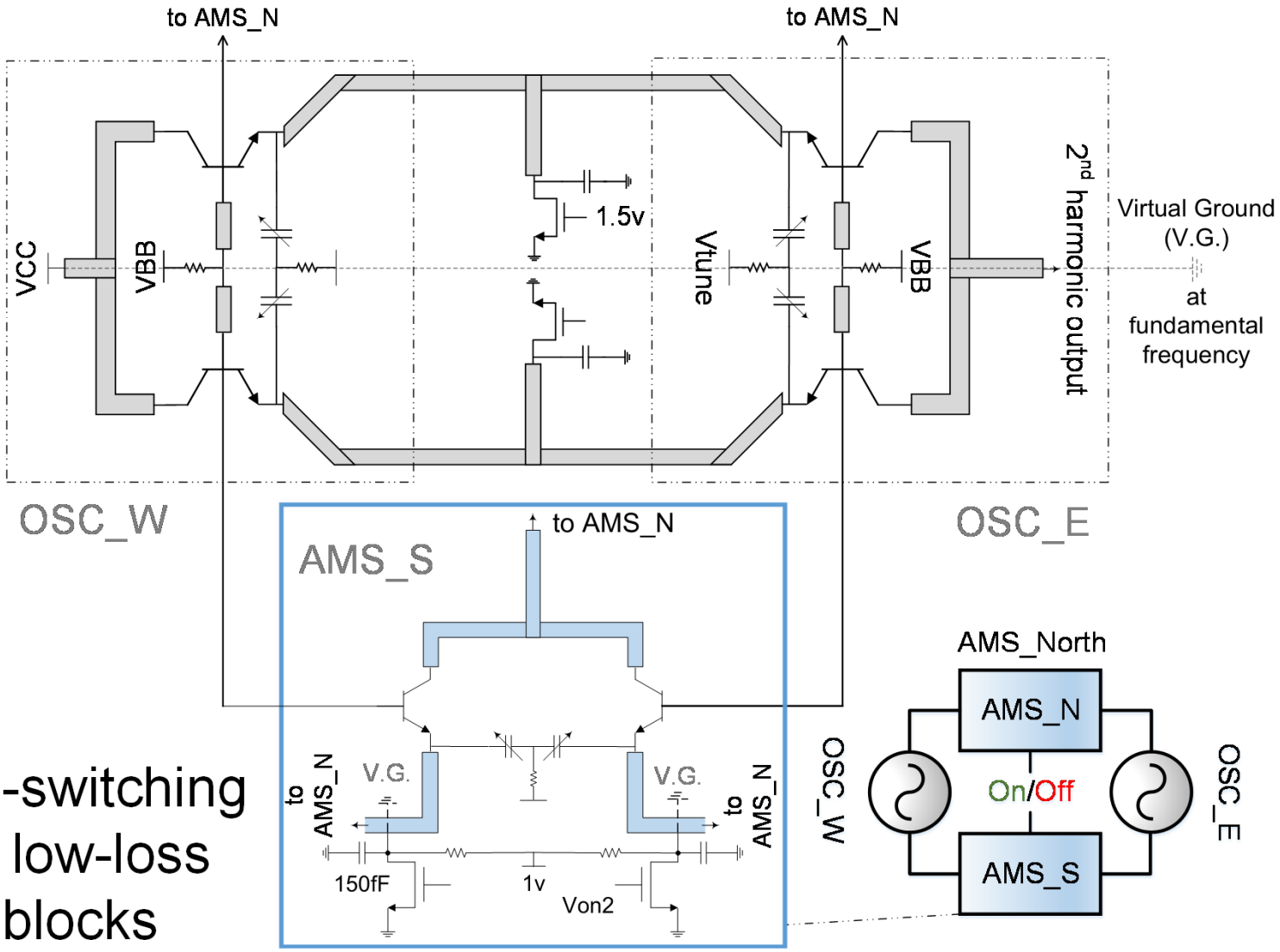
- Core VCO with more than 10% of tuning range
  - Colpitts structure
  - Varactors are in emitters
  - Varactors are not in the harmonic extraction path
  - Extended tuning range using **HBTs**

Coupled Core VCOs



Coupling two identical VCOs through emitter lines

AMS Block

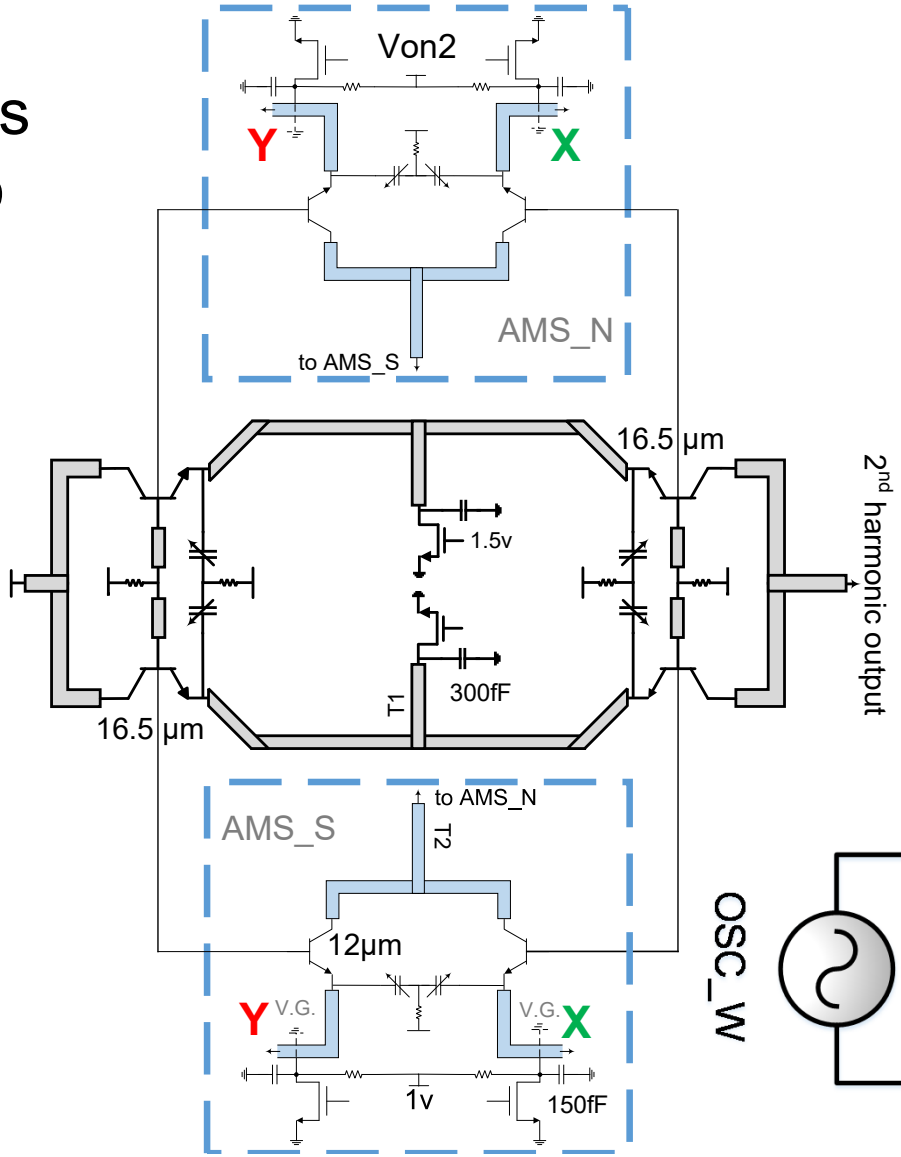


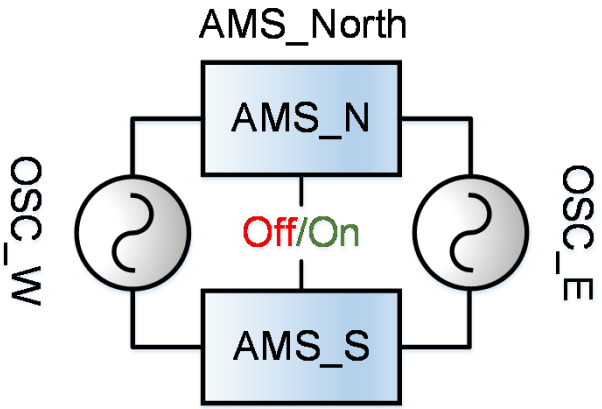
Mode-switching using low-loss **AMS** blocks

Active Mode Switching

Complete Mode-Switching VCO

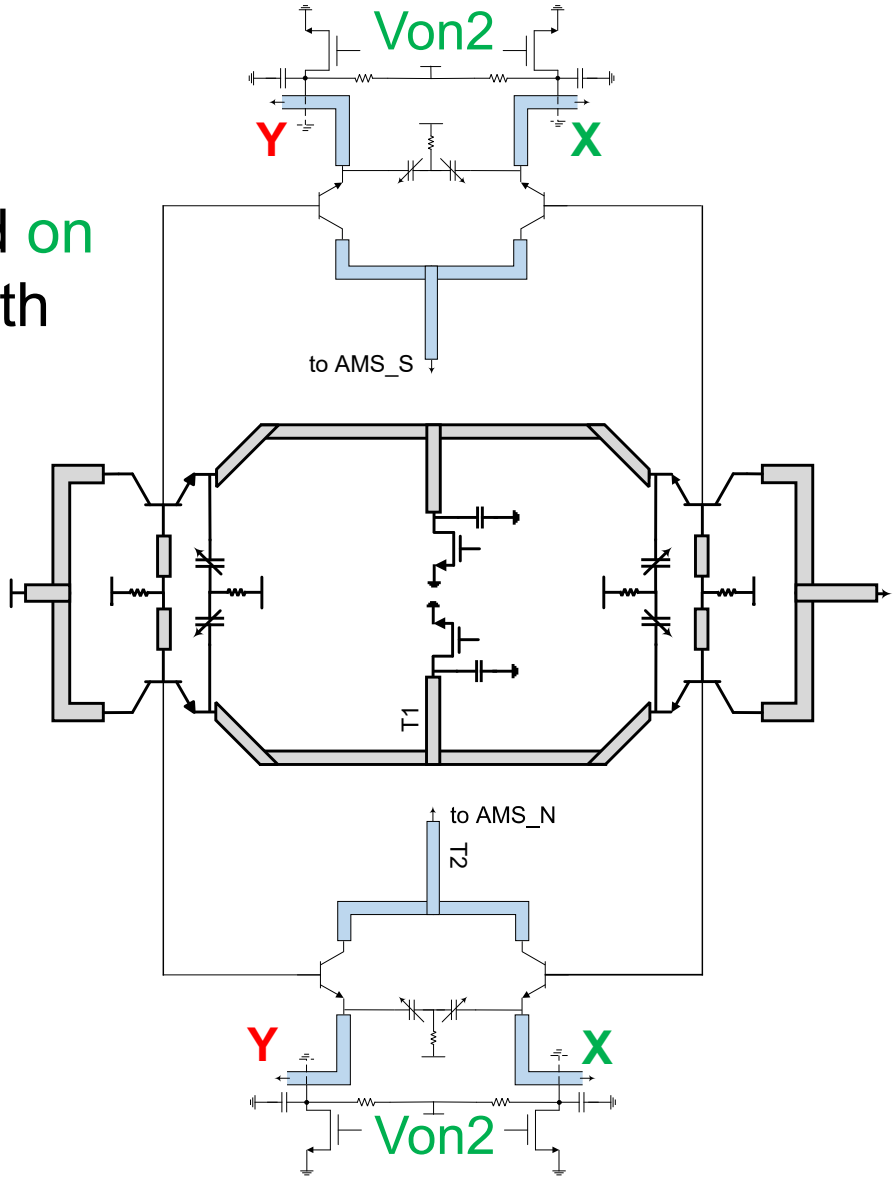
Nodes X and nodes Y are connected to each other





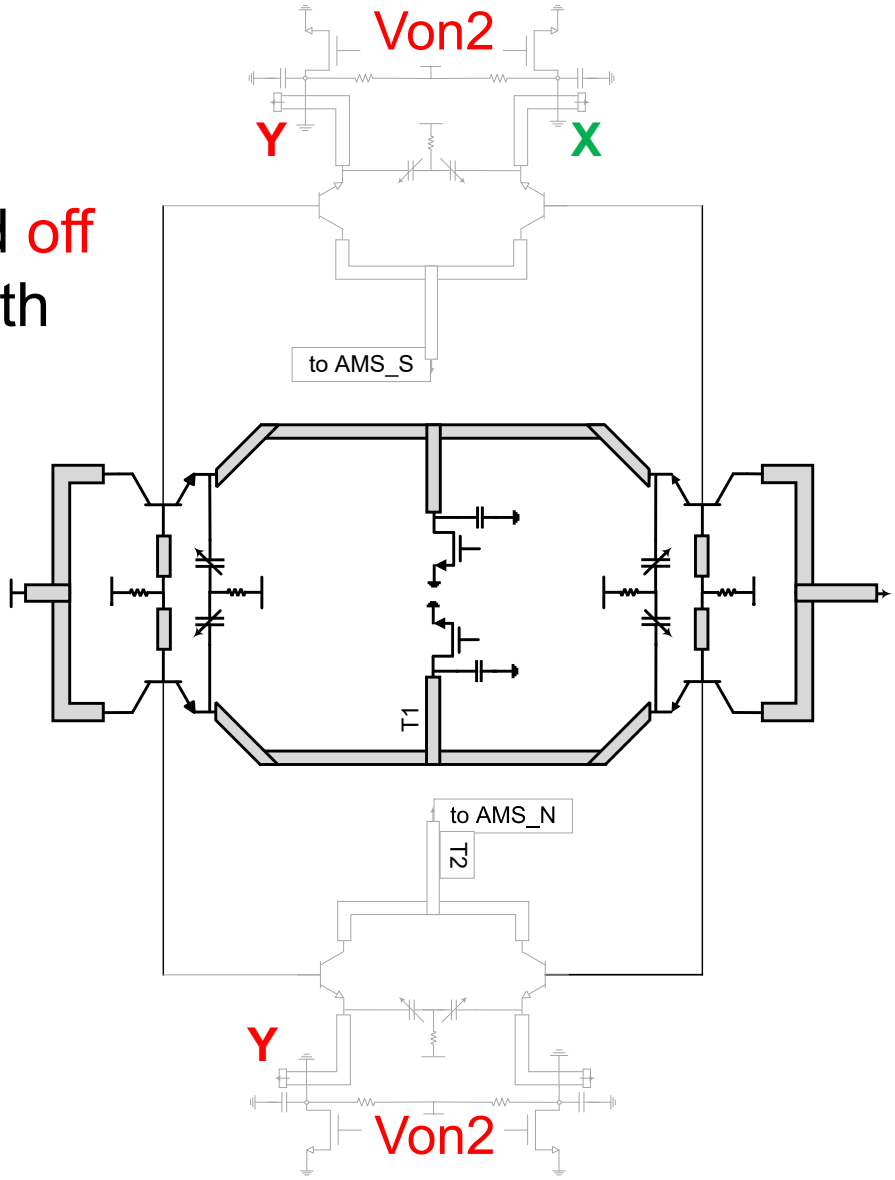
Odd Mode

- Von2 = 1.2V
  - AMS blocks are turned on
  - They load the tanks with high capacitance
- Lower frequency of oscillation



Even Mode

- Von2 = 0V
  - AMS blocks are turned off
  - They load the tanks with low capacitance
- Higher frequency of oscillation

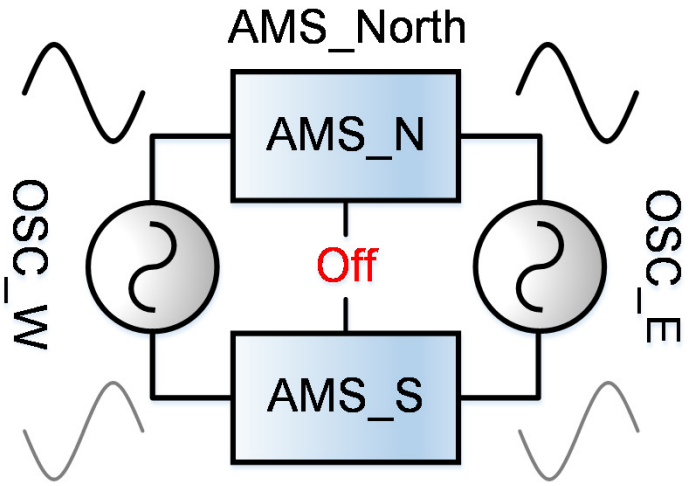


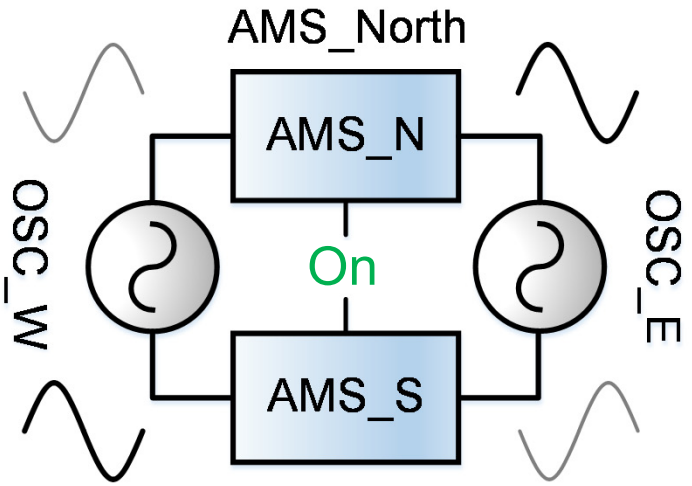
Outline

- Motivation
- Mode-switching VCO Circuit Architecture
- **Modes of Operation**
- Measurement Results
- Conclusion

Modes of Operation

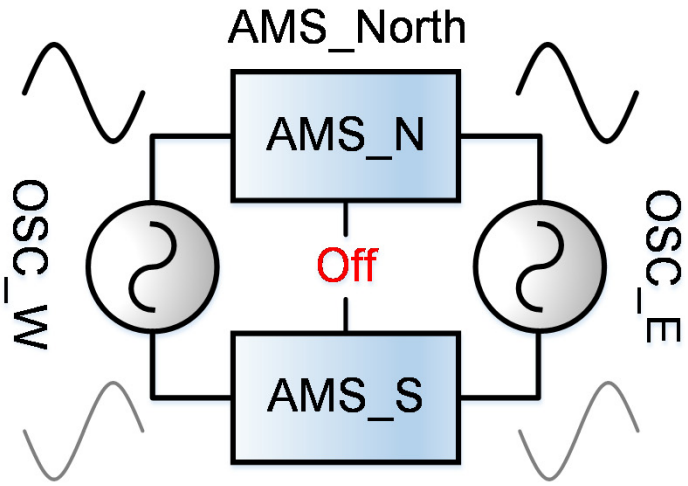
- Even mode
  - In-phase oscillation
- Odd mode
  - Out-of-phase oscillation

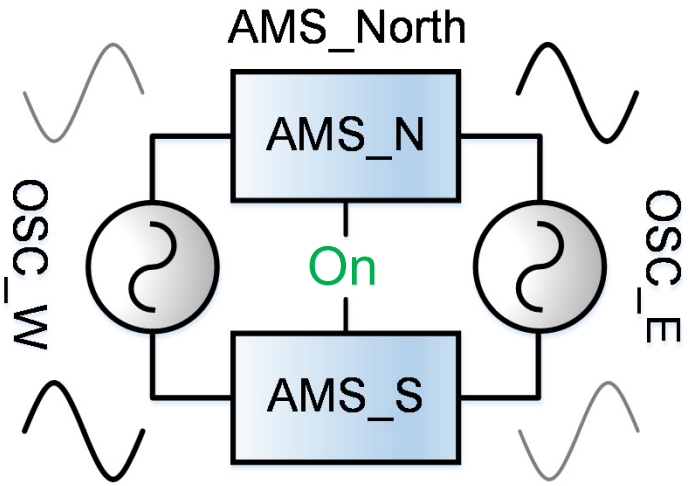




Modes of Operation

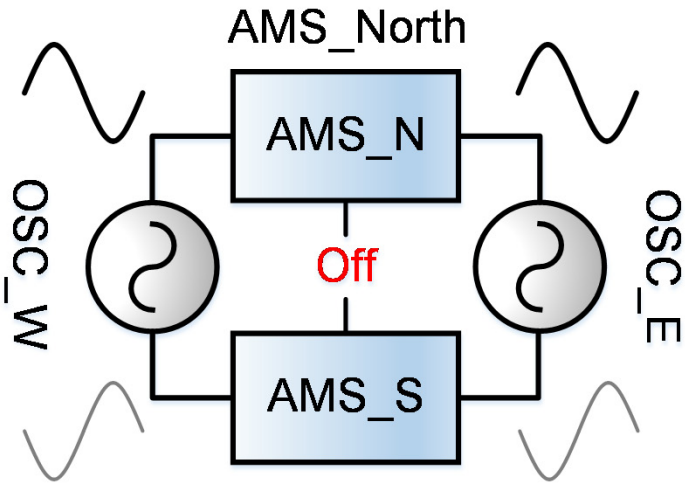
- Even mode
  - In-phase oscillation
  - Higher center frequency
- Odd mode
  - Out-of-phase oscillation
  - Lower center frequency

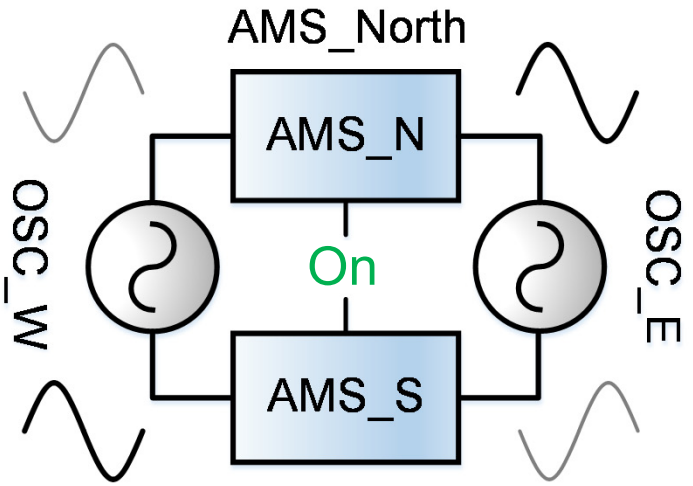




Modes of Operation

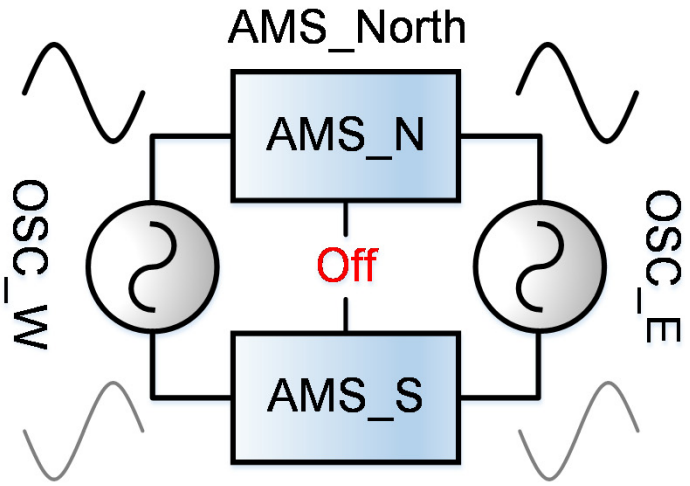
- Even mode
  - In-phase oscillation
  - Higher center frequency
  - AMS blocks are low-loss
- Odd mode
  - Out-of-phase oscillation
  - Lower center frequency
  - AMS blocks cancel loss

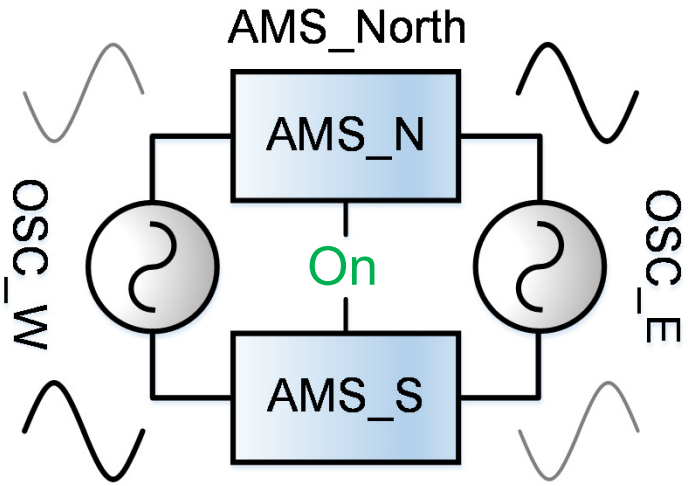




Modes of Operation

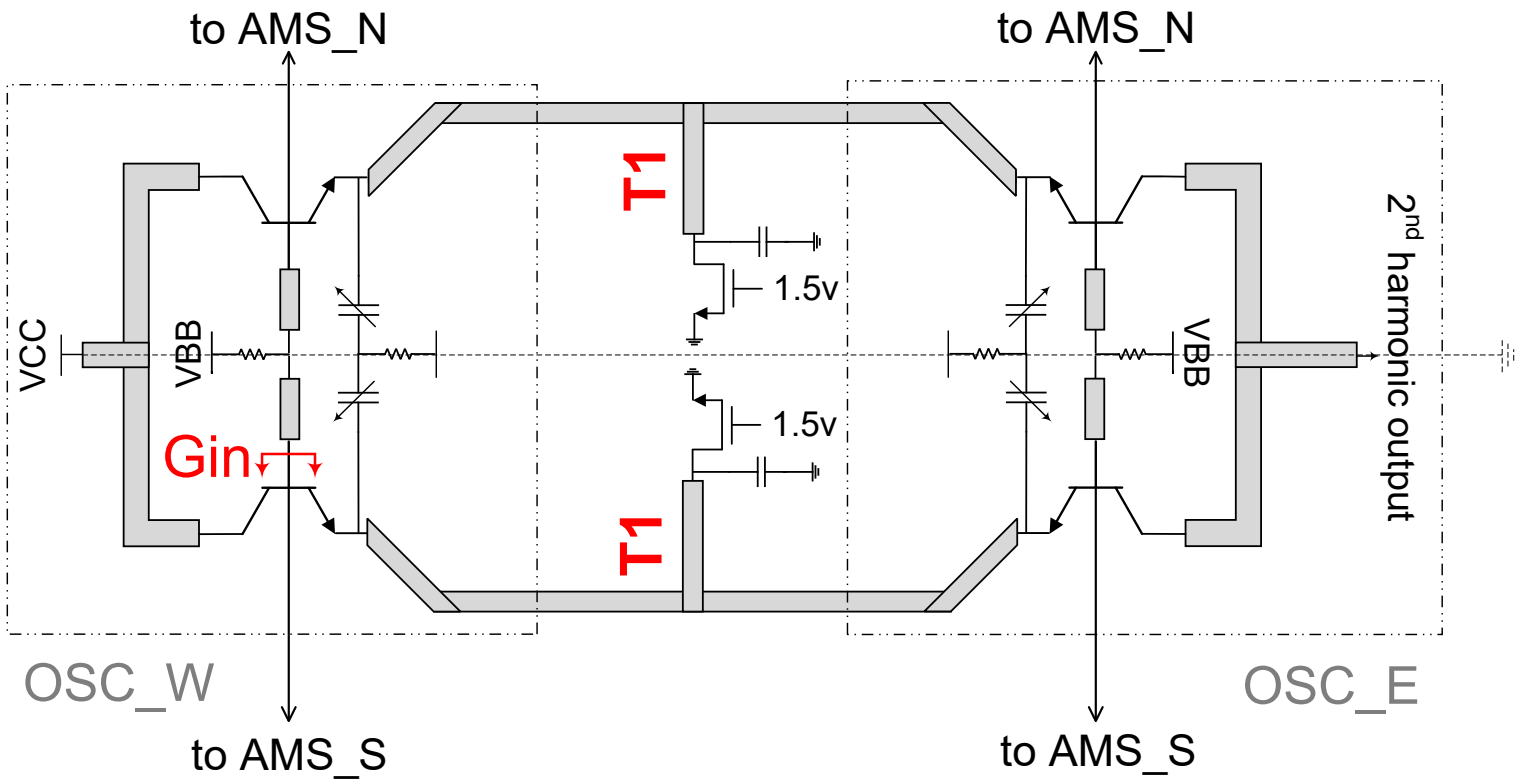
- Even mode
  - In-phase oscillation
  - Higher center frequency
  - AMS blocks are low-loss
  - AMS blocks are low-Cap.
- Odd mode
  - Out-of-phase oscillation
  - Lower center frequency
  - AMS blocks cancel loss
  - AMS capacitance is tunable





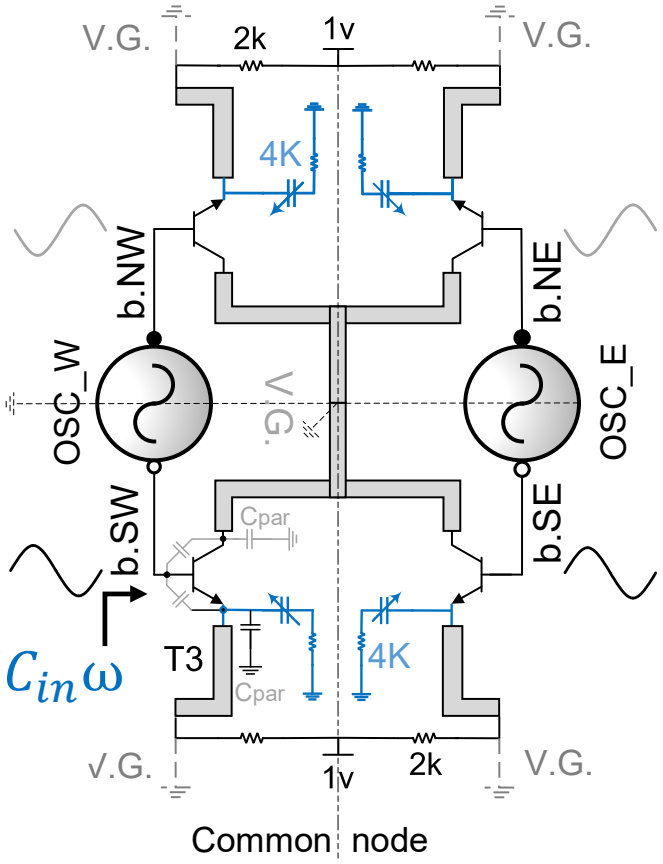
Even Mode: In-phase Operation

- AMS blocks are turned-off
- T1 forces oscillation to be in-phase
- T1 helps with stronger oscillation

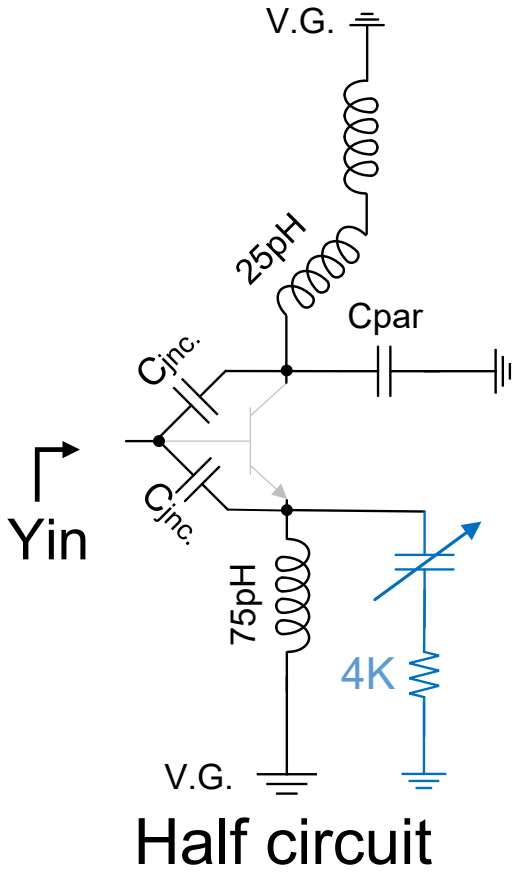


Even Mode: AMS Equivalent Circuit

- In-phase oscillation
  - Varactors are in series with 4kΩ resistors
  - Varactors loadings on the tanks are reduced



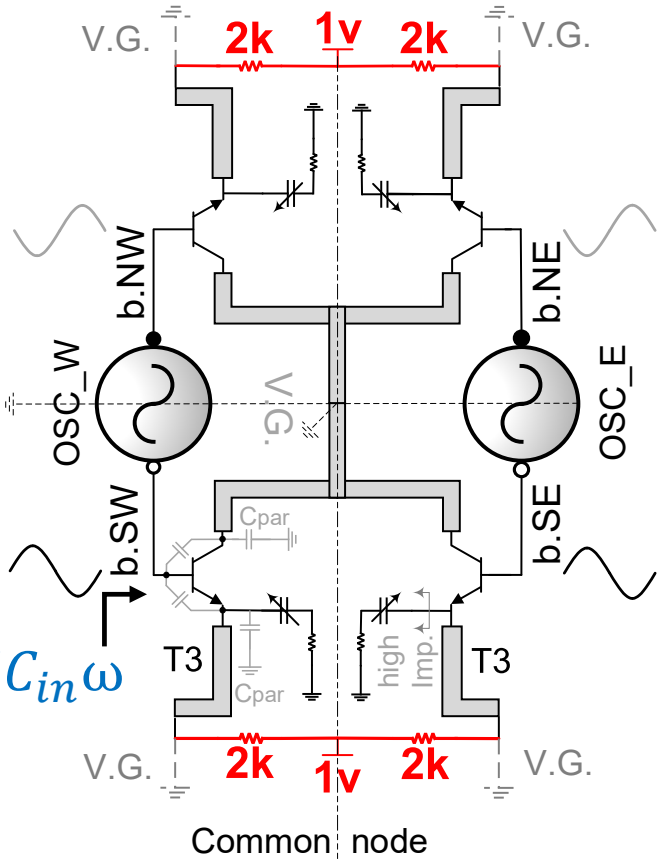
$$Y_{in} = G_{in} + jC_{in}\omega$$

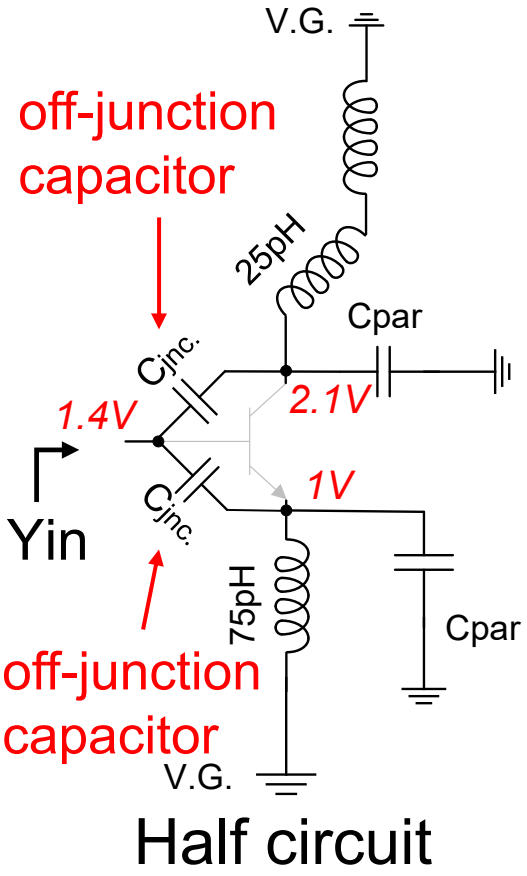


Even Mode: AMS Equivalent Circuit

- Emitter voltages are raised to 1V
  - AMS is off
  - Off-Junction capacitors reduce tank loading

$$Y_{in} = G_{in} + jC_{in}\omega$$

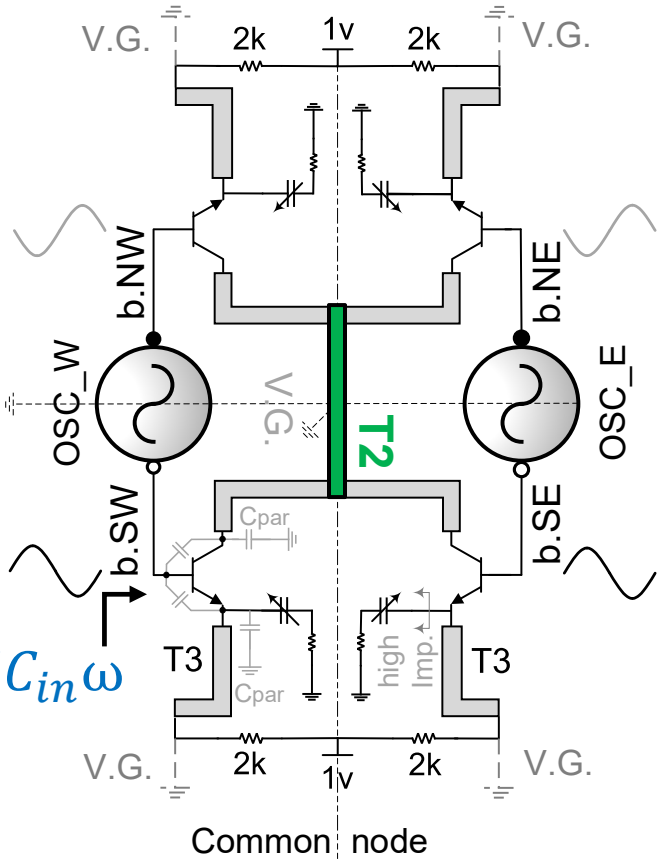




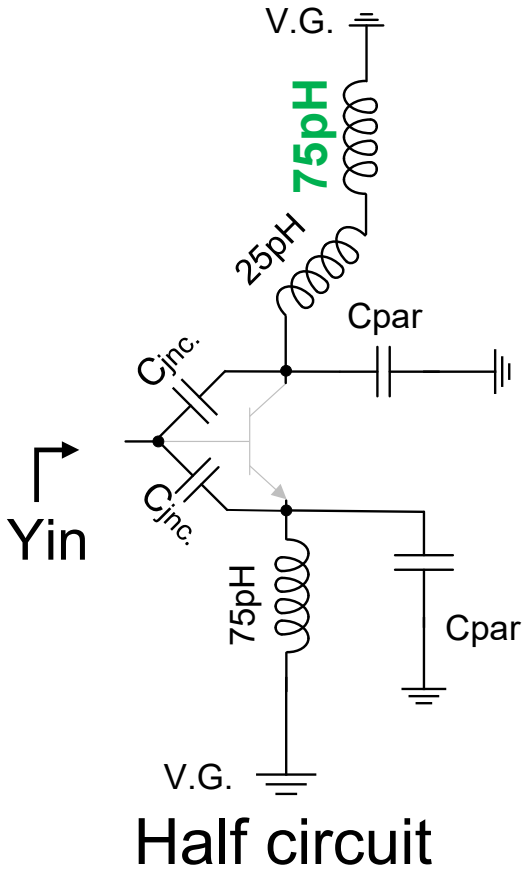
Half circuit

Even Mode: AMS Equivalent Circuit

- In-phase oscillation increases the inductance connected to the collector
- They resonate with the parasitic capacitors



$$Y_{in} = G_{in} + jC_{in}\omega$$



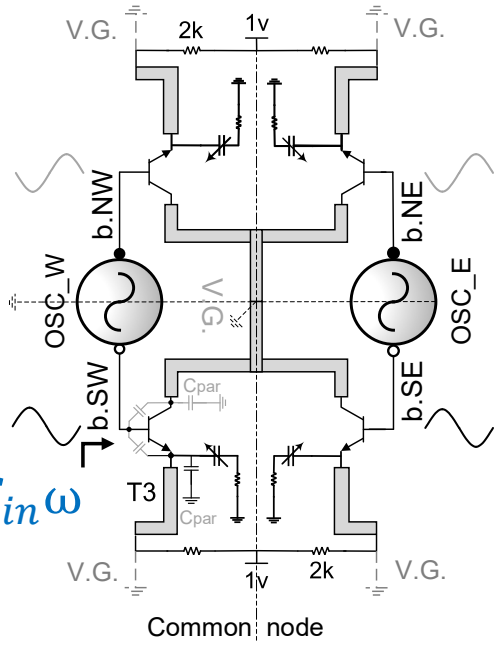
Half circuit

Even Mode: AMS Loading on Tank

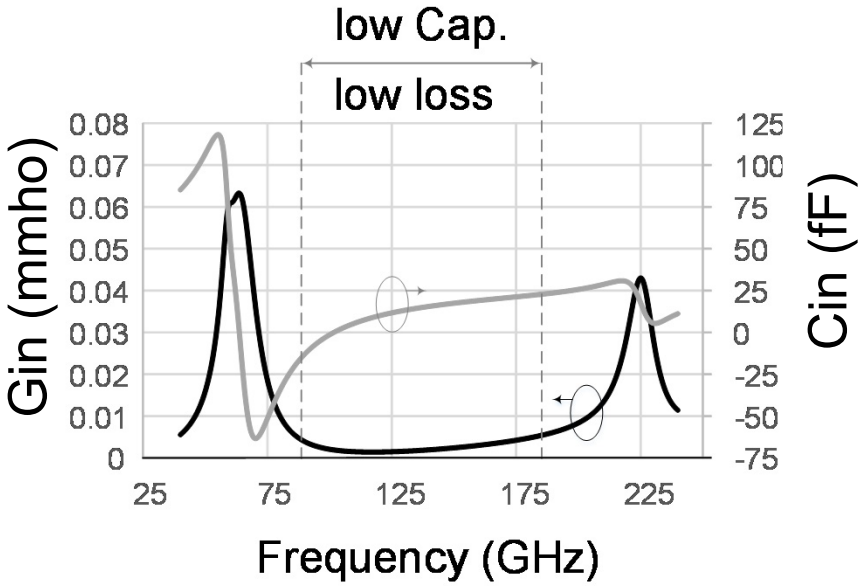
- Large inductors at collector and emitter
- Small off Junction Capacitors
- Large resistors in series with the varactors

➡ They lower the loss and capacitance loading of the AMS blocks

Tuning range, output power and frequency are kept high



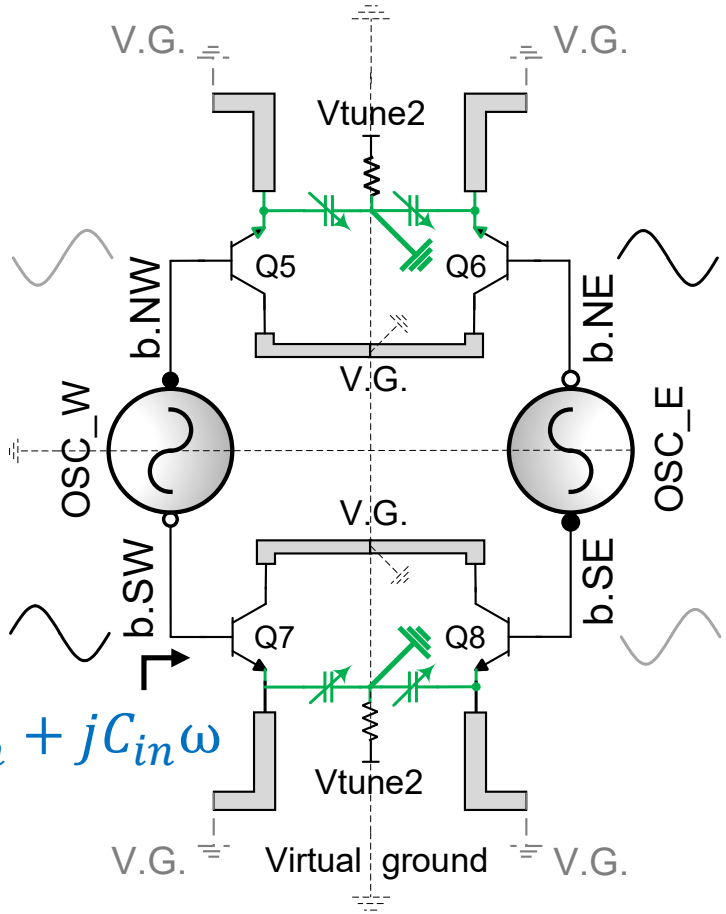
$G_{in} + jC_{in}\omega$



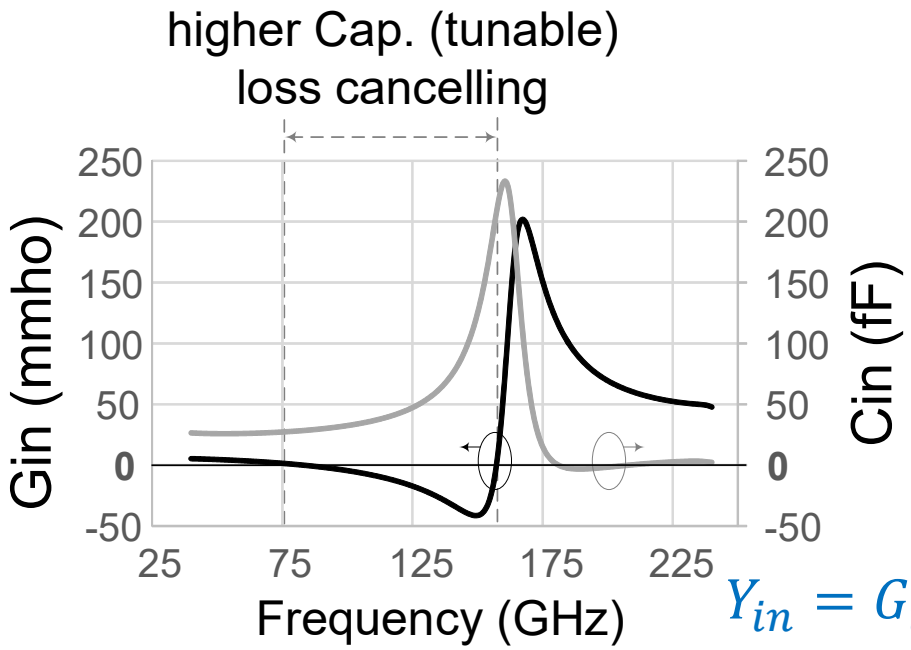
Odd Mode: AMS Equivalent Circuit

- AMS is on
- With out-of-phase oscillation, varactors are seen from the tanks
  - AMS transistors are now Colpitts embedded
  - AMS cancels loss at tank
  - varactors contribute to frequency tuning

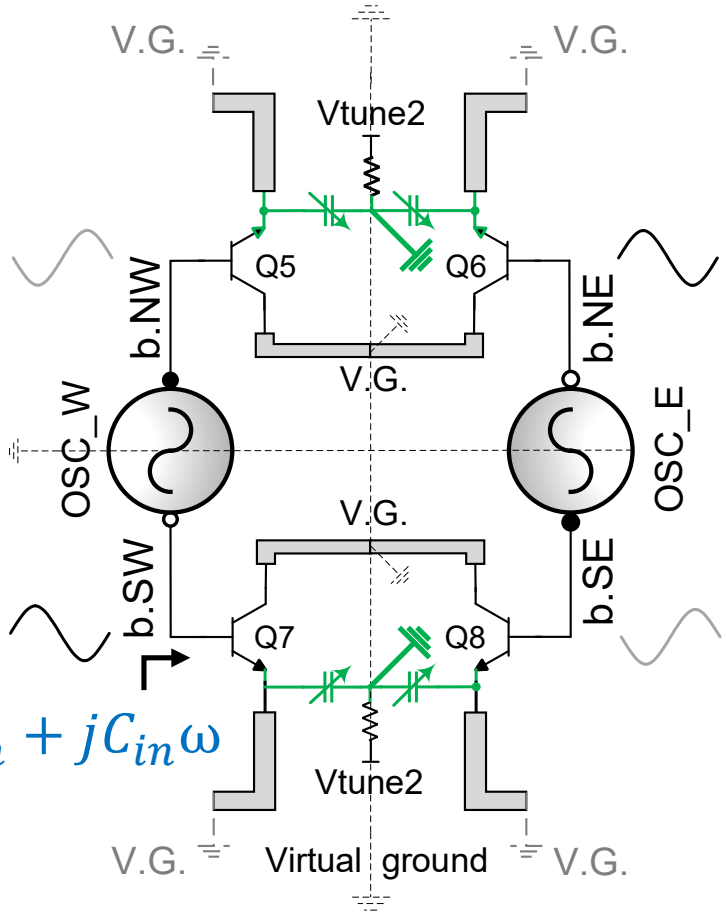
$$Y_{in} = G_{in} + jC_{in}\omega$$



Odd Mode: AMS Equivalent Circuit

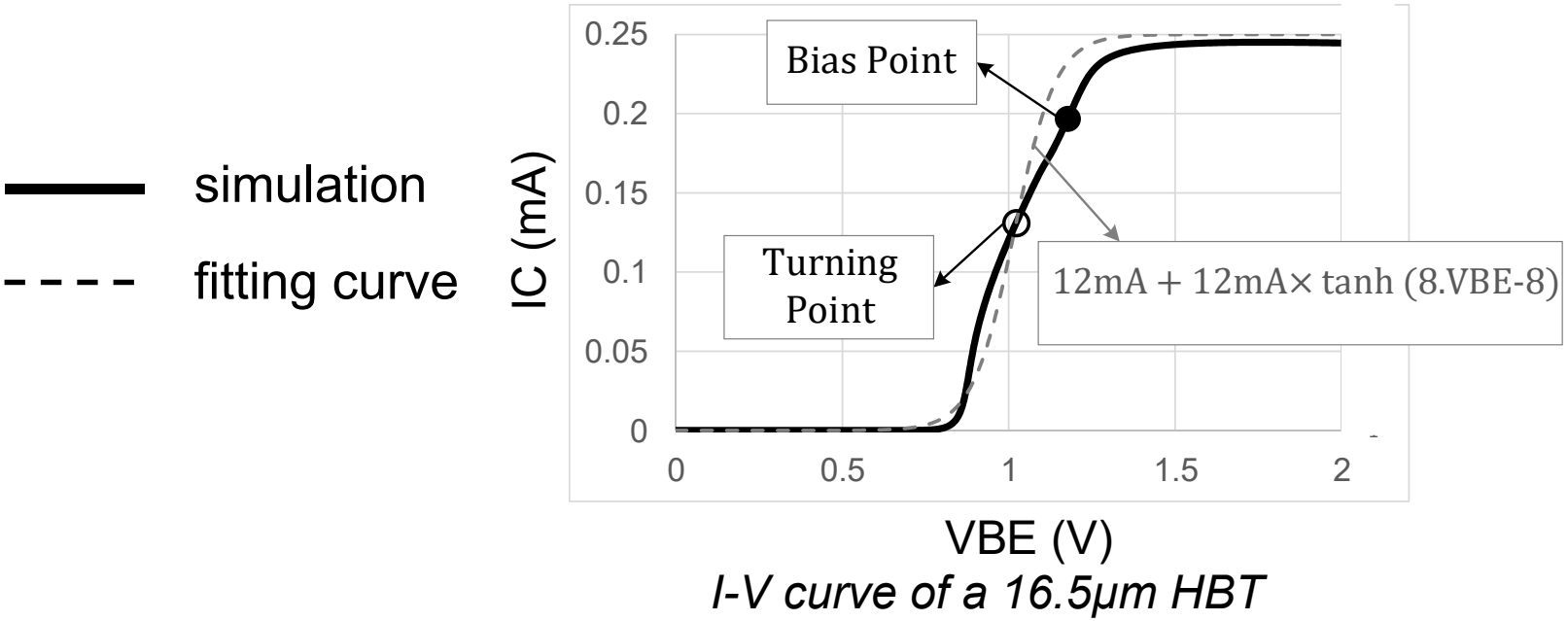


$$Y_{in} = G_{in} + jC_{in}\omega$$



Output Power Improvement

- Power extracted from only one of the core VCOs
- Only odd harmonics are generated at turning point
- Transistors are Biased away from the turning point
- Varactors are not in harmonic extraction path



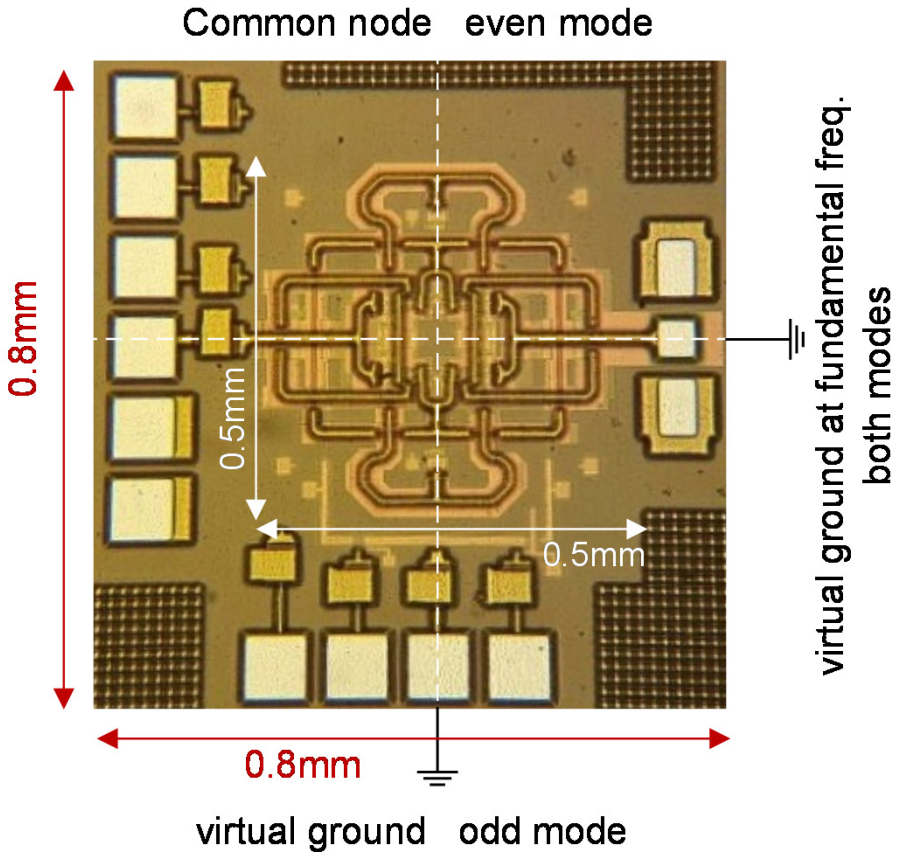
I-V curve of a 16.5μm HBT

Outline

- Motivation
- Mode-switching VCO Circuit Architecture
- Modes of operation of the VCO
- **Measurement Results**
- Conclusion

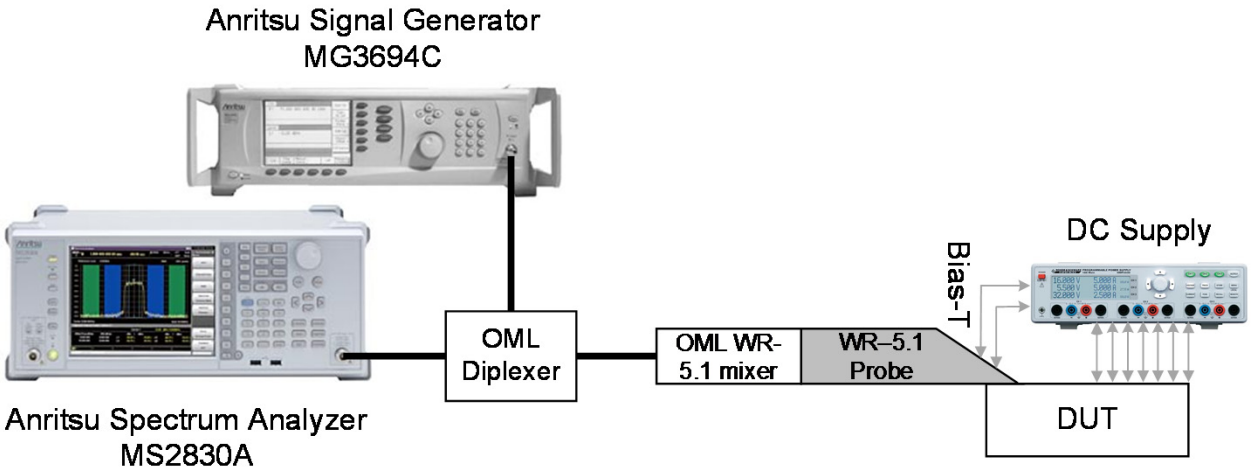
Chip Photo

- Designed and implemented in IBM 0.13µm BiCMOS process
- All the lines are microstrip using top two metal layers and were fully simulated



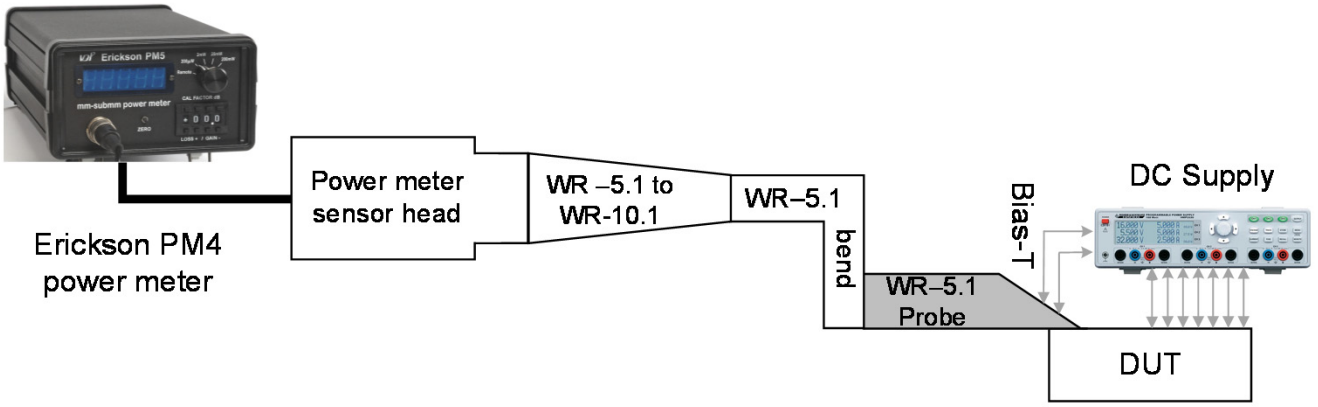
Measurement Setup

Down-converting
by Harmonic mixer



Frequency Measurement Setup

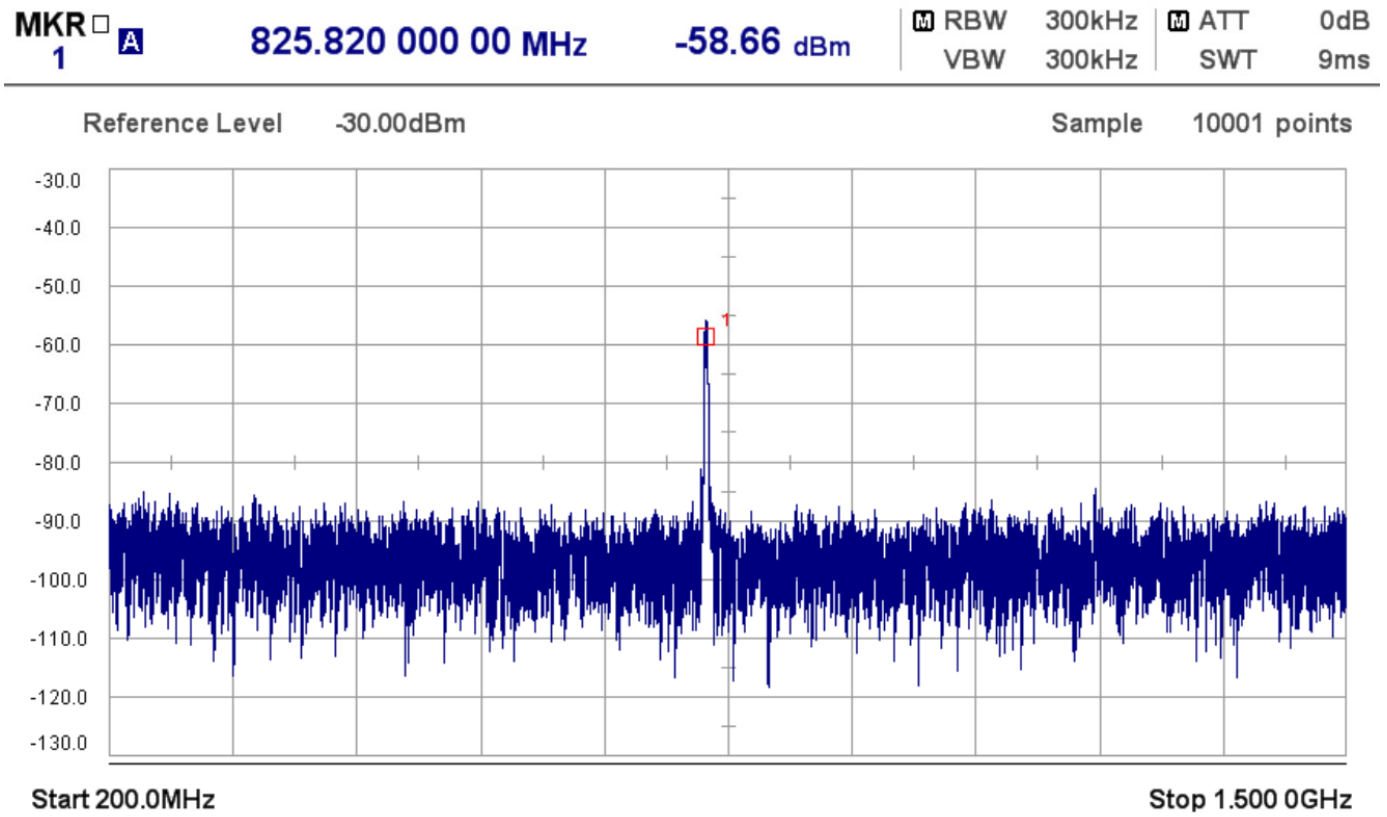
Erikson PM4
power meter



Power Measurement Setup

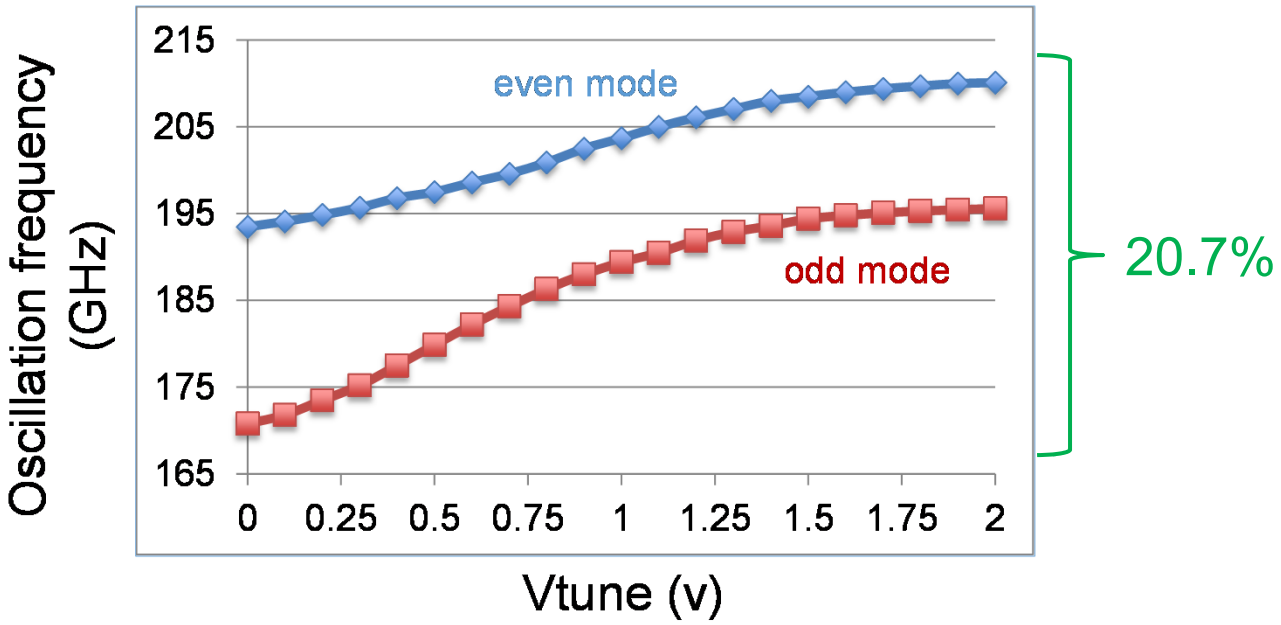
Output Spectrum

- 210.1GHz Signal was down-converted by the 12th harmonic of the mixer.



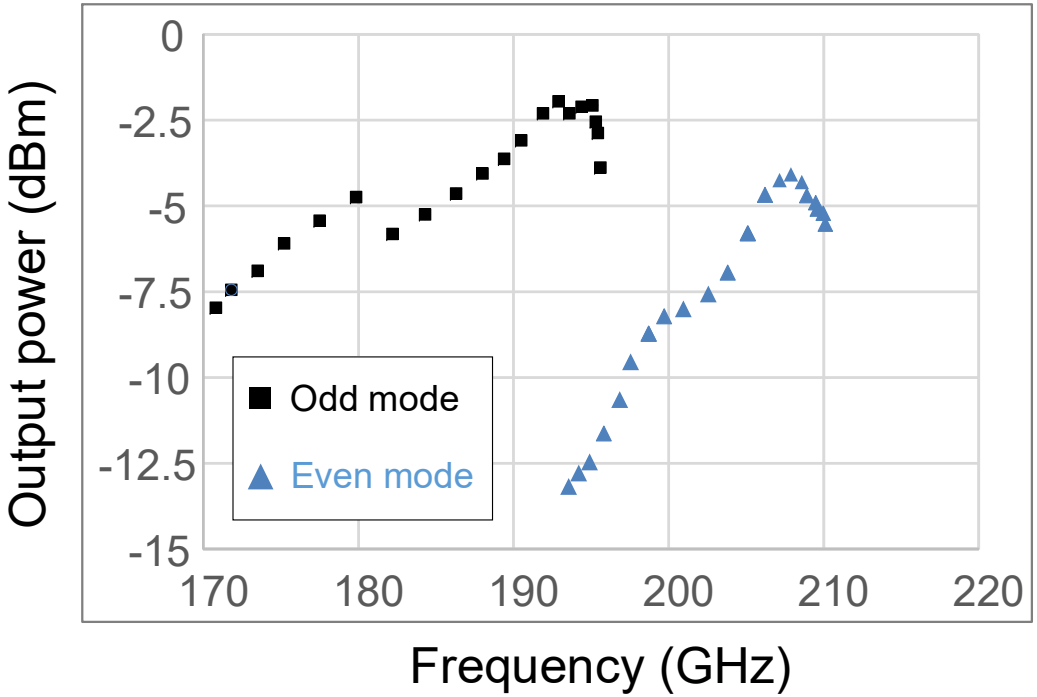
Measured Frequency Range

- Even Mode
  - 193.5GHz – 210.1GHz
  - 8.3% of tuning range
- Odd Mode
  - 170.8GHz – 195.6GHz
  - 13.6% of tuning range



Measured Power

- AMS loads the tanks with low-loss in even mode
- AMS cancels loss in odd mode
  - Odd mode has more output power
  - Maximum output power of -2.1dBm at 193GHz



Measured Phase Noise as a Function of Frequency

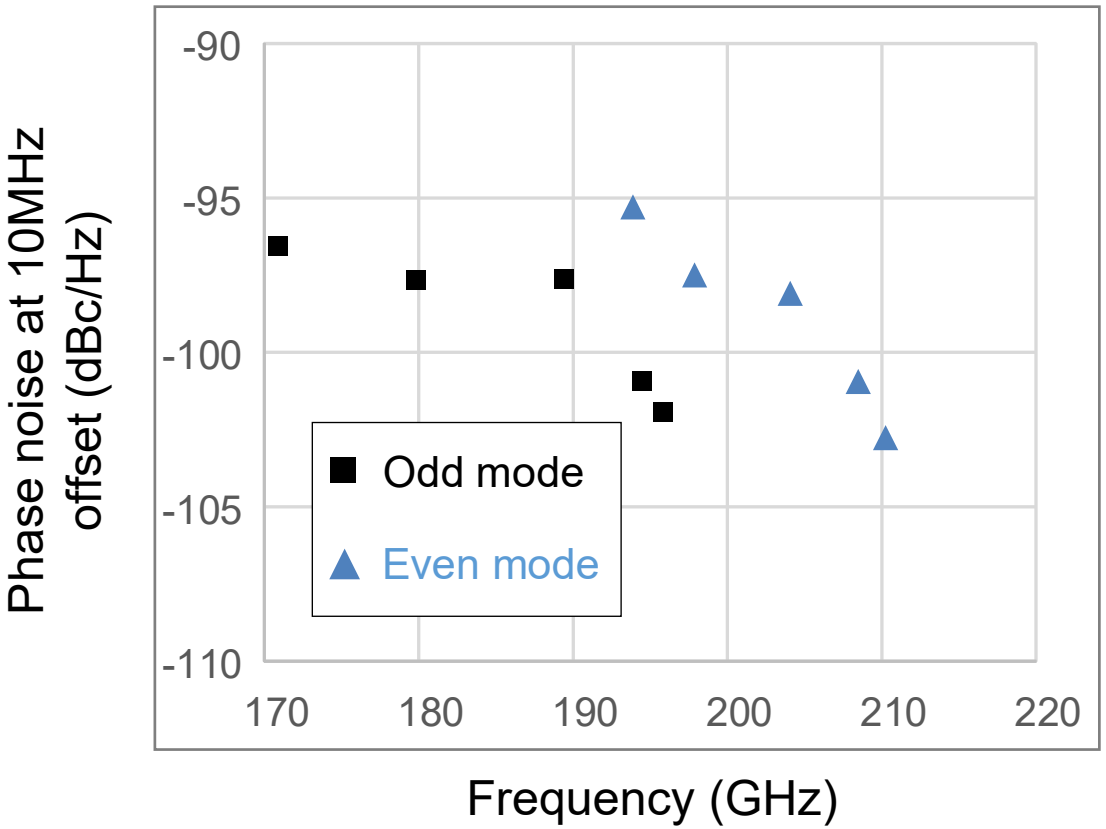


Table of Comparison

Reference	[1]	[2]	[3]	[4]	[5]	[6]	**This Work**
Center Freq. (GHz)	106.7	256	290	239	260	290	**190.5**
Tuning Range (%)	39.4	4.3 (6.5*)	4.5	12.5	1.4 (9.5**)	8	**20.7**
Fundamental Freq. (GHz)	26.7	128	72.5	119.5	130	96.7	**95.25**
Max. Output Power (dBm)	-15	4.1	-1.2	-4.8	0.5	-14	**-2.1**
Max. DC Power (mw)	45	227	325	18.5	800	105.6	**294 (Odd mode) 183 (even mode)**
Best Phase Noise (dBc/Hz)	-108.2 @10MHz	-94 @1MHz	-78 @1MHz	-110.9 @10MHz	-78 @1MHz	-80.28 @1MHz	**-102.64 @10MHz**
Technology, f_{max} (GHz)	65nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	90nm BiCMOS 315GHz	**130nm BiCMOS 210GHz**
Measurement	Probing	Probing	Probing	Probing	Radiation	Probing	**Probing**

* Including frequency tuning by change of supply voltage.

** Pulse modulation for broadband radiation. Not continuous frequency tuning.

Outline

- Motivation
- Mode-switching VCO Circuit Architecture
- Modes of operation of the VCO
- Measurement Results
- **Conclusion**

Conclusion

- A mode-switching VCO to achieve wide tuning range was presented

- Active Mode Switching blocks (AMS) coupled two Colpitts oscillators
- In-phase Vs. out-of-phase operation

  - Low-loss mode switching ➡ High output power
  - Low-Cap. mode switching ➡ Wide tuning range

Acknowledgements

- National Science Foundation (NSF) for supporting this project
- Cascade Microtech for measurement support
- Mr. Hossein Jalili and all lab members

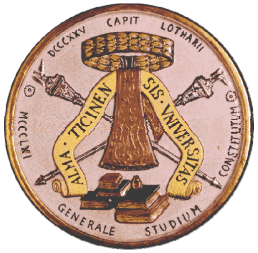
A 0.003mm^2 1.7-to-3.5GHz Dual-Mode Time-Interleaved Ring-VCO Achieving 90-to-150kHz 1/f^3 Phase-Noise Corner

Jun Yin [1], Pui-In Mak [1], Franco Maloberti[2] and Rui P. Martins[1,3]

1 – State-Key Laboratory of Analog and Mixed-Signal VLSI
University of Macau, Macao SAR, China

2 – University of Pavia, Pavia, Italy

3 – Instituto Superior Técnico, Universidade de Lisboa, Portugal

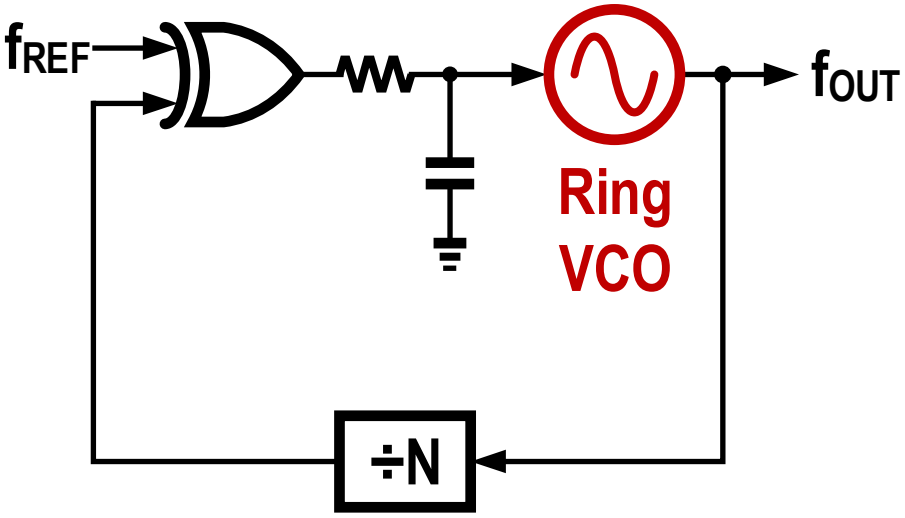


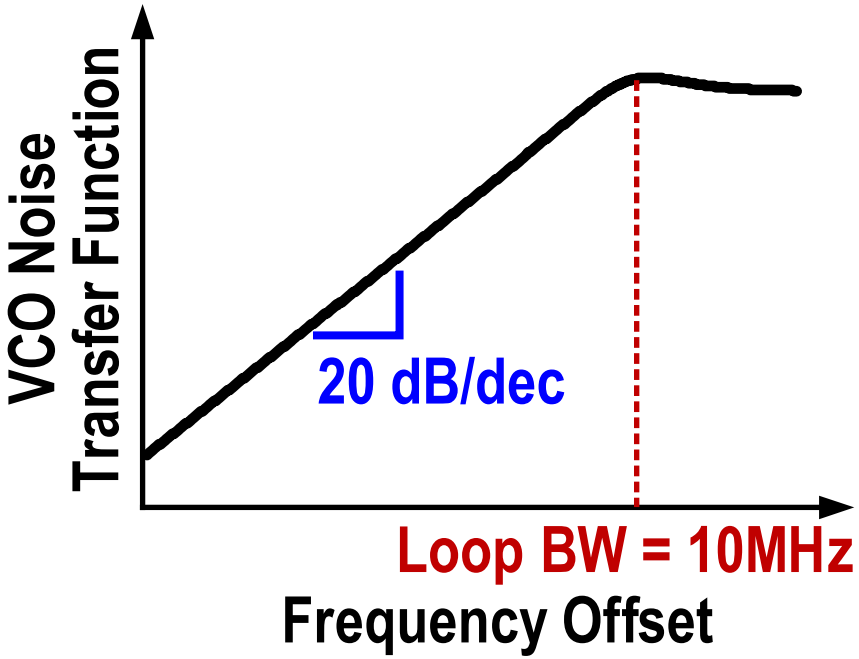
Outline

- **Motivation**
- **Proposed time-interleaved Ring-VCO (TI-RVCO)**
- **Experimental results**
- **Comparison with the prior art**

Motivation (1)

Type-I PLL Using Ring VCO [L. Kong et. al., ISSCC'15]





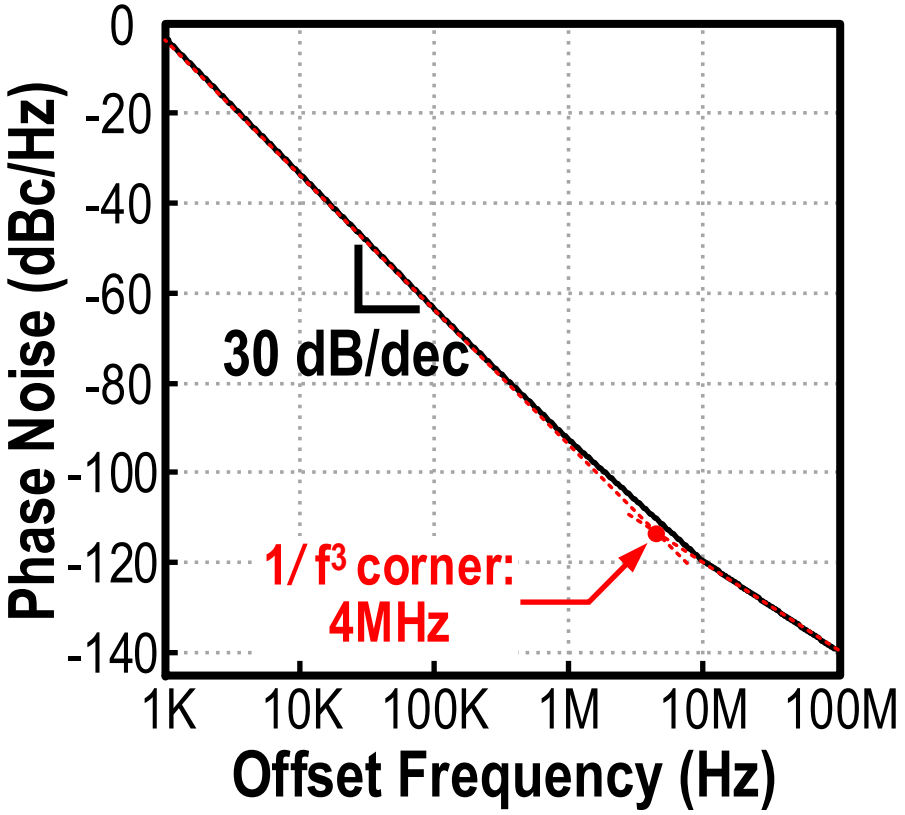
- **Inductorless RF frequency synthesizer for WLAN**

☑ **Large Loop BW to suppress RVCO Phase Noise**

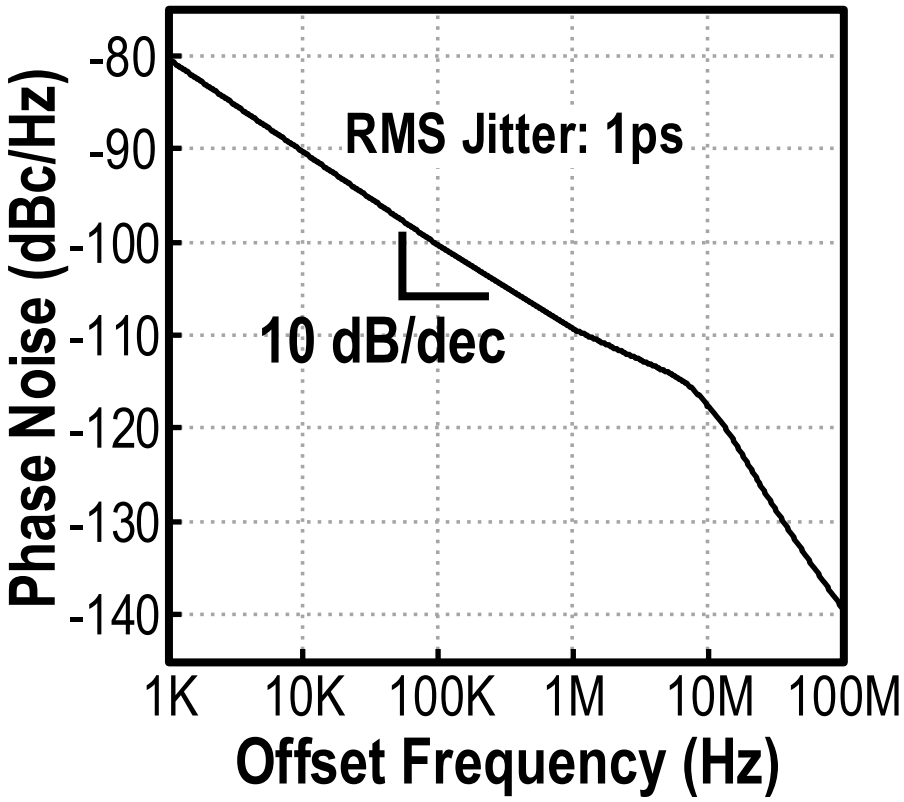
☑ **Area, tuning range and no magnetic coupling**

Motivation (2)

Ring VCO



Type-I PLL

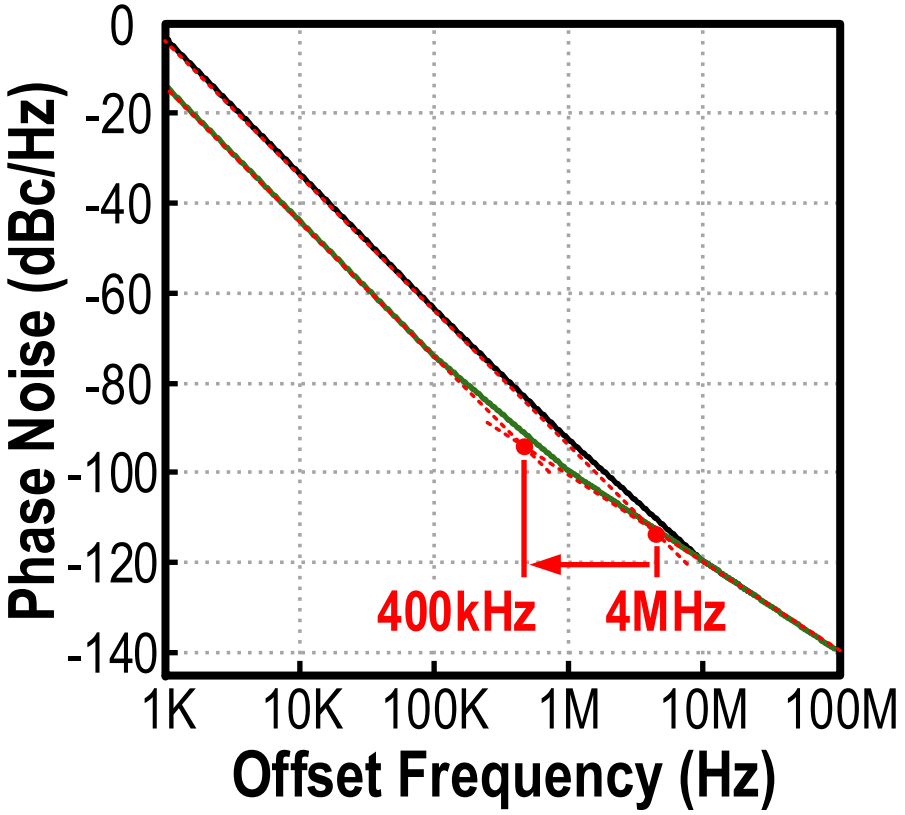


☒ Large 1/f³ Phase Noise corner of RVCO (~MHz)

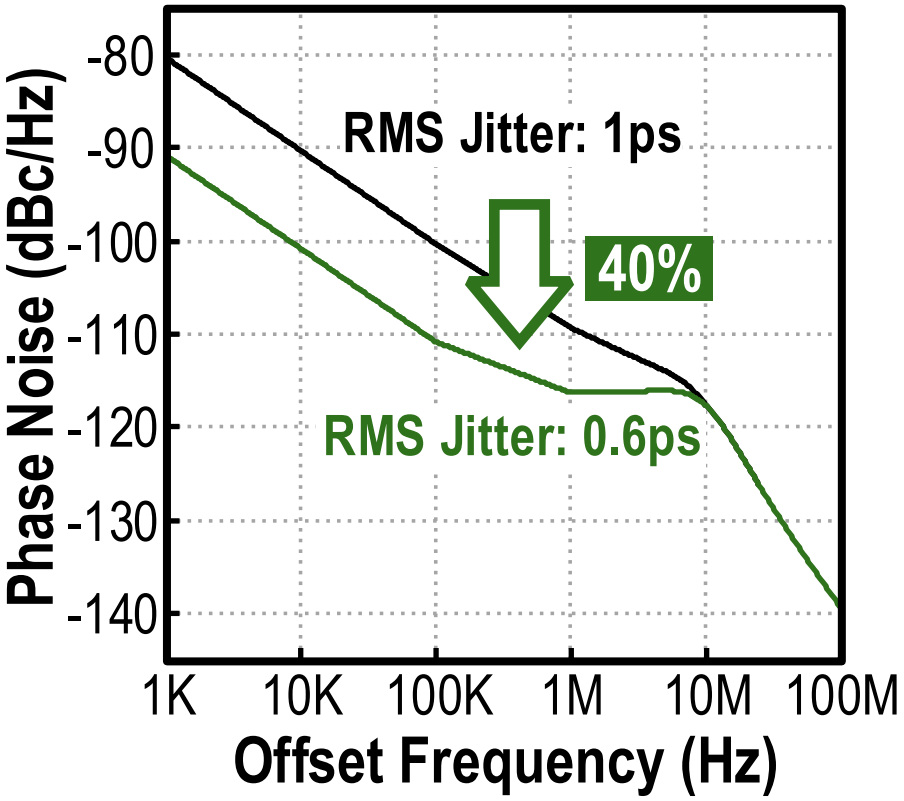
➔ **Large in-band Phase Noise & jitter**

Motivation (2)

Ring VCO



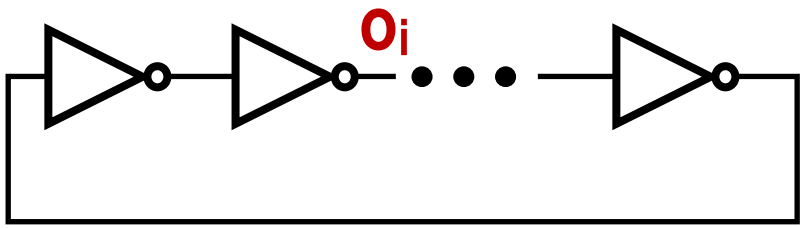
Type-I PLL

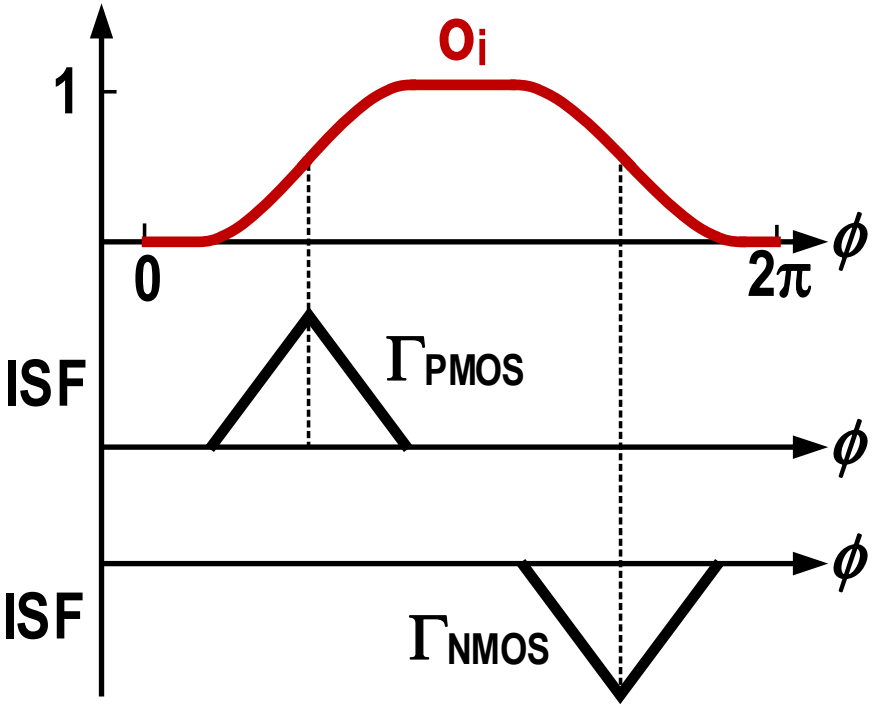


☒ Large $1/f^3$ Phase Noise corner of RVCO (~MHz)

➔ **Large in-band Phase Noise & jitter**

$1/f^3$ Corner of Ring VCO





Assumptions

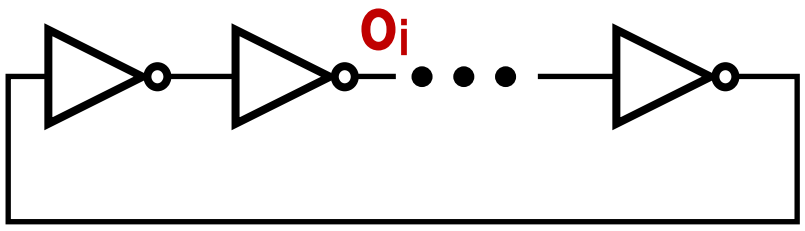
1. 1/f noise generated by NMOS and PMOS are uncorrelated

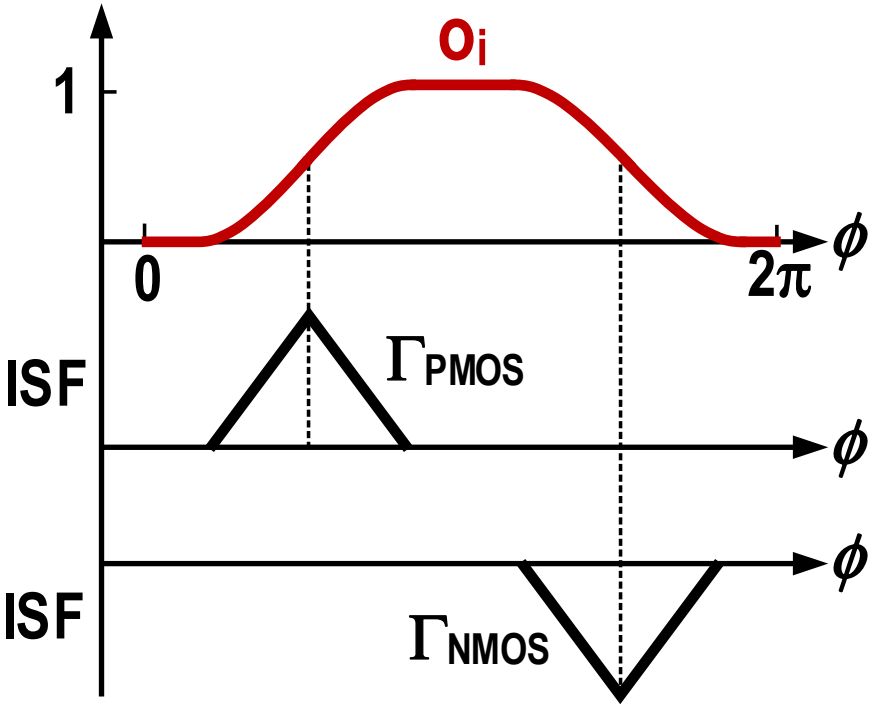
2. Same $f_{1/f}$ for NMOS and PMOS

$$f_{1/f^3} = f_{1/f} \frac{\left(|\Gamma_{NMOS,DC}| + |\Gamma_{PMOS,DC}|\right)^2}{\Gamma_{NMOS,rms}^2 + \Gamma_{PMOS,rms}^2}$$

[A. Hajimiri et. al., JSSC'99]

$1/f^3$ Corner of Ring VCO





Assumption

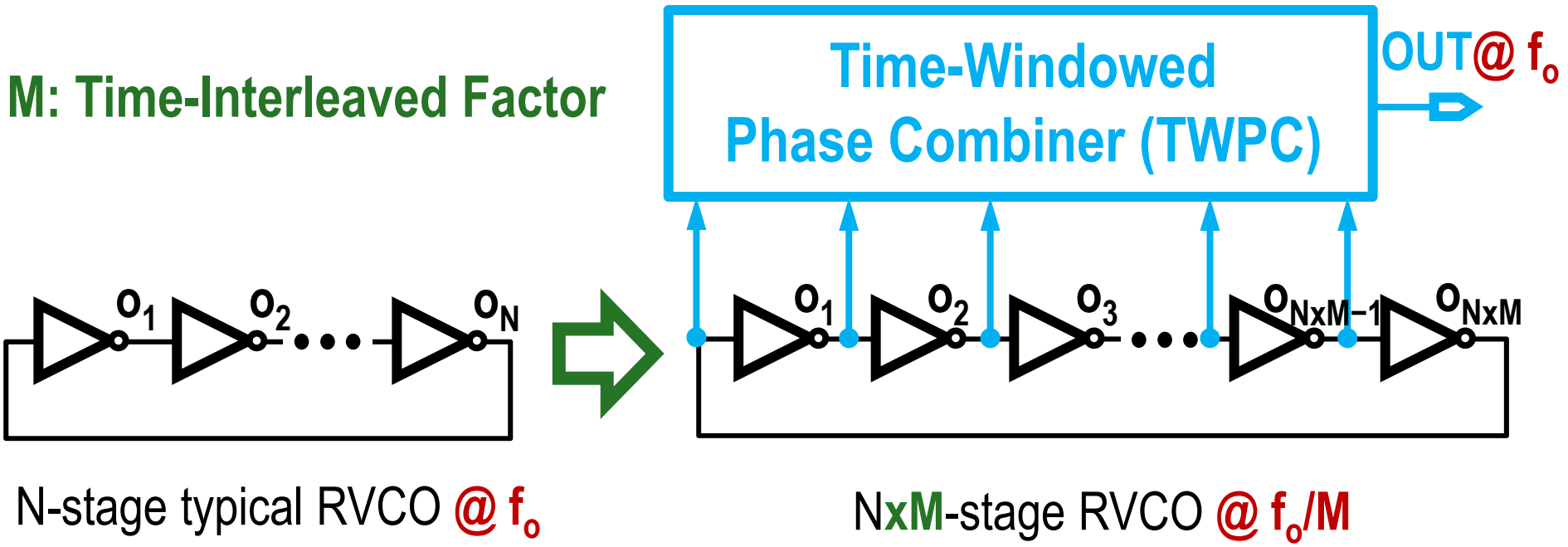
Rising and falling edges are symmetrical:

$$|\Gamma| = |\Gamma_{NMOS}| = |\Gamma_{PMOS}|$$

$$f_{1/f^3} = f_{1/f} \frac{3}{4\eta} \times \frac{1}{\text{No. of Stage}}$$

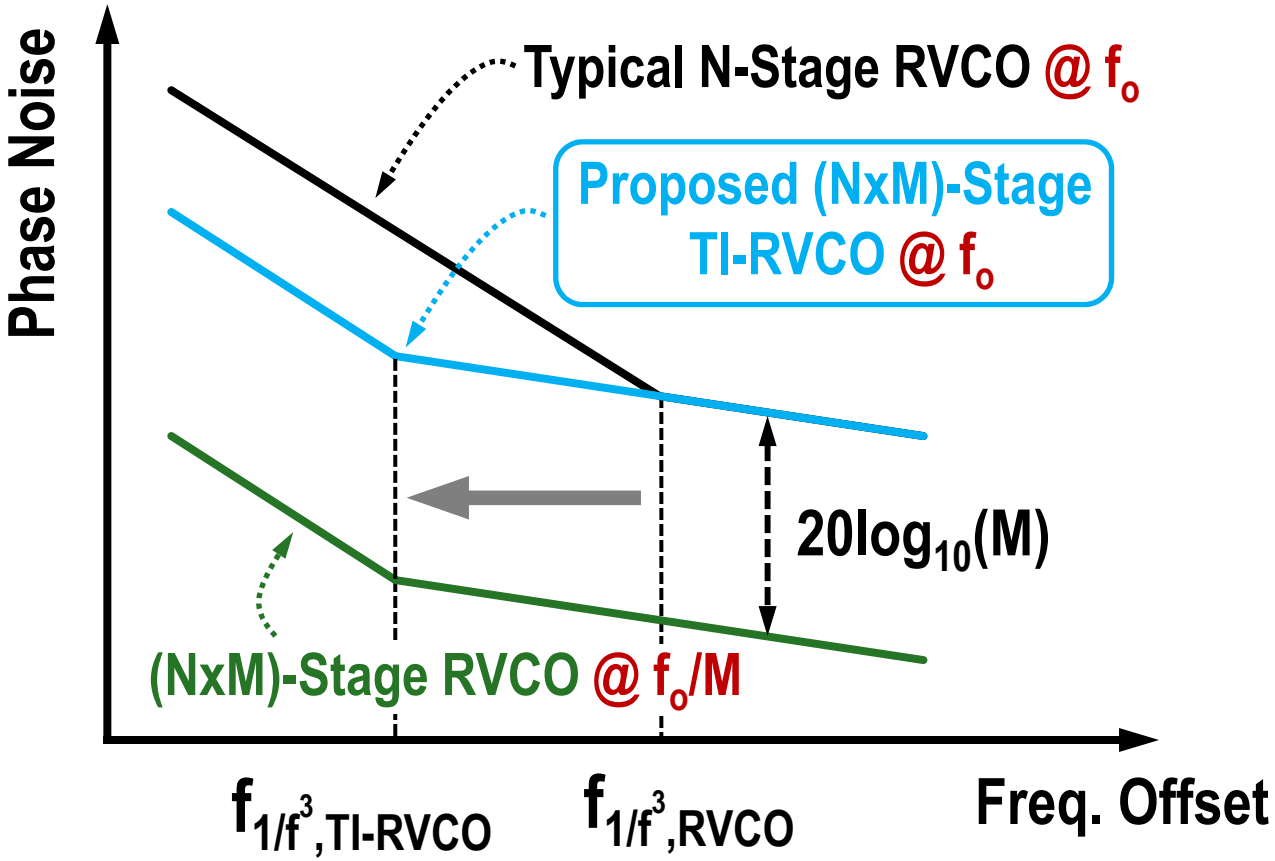
[A. Hajimiri et. al., JSSC'99]

Concept of the Proposed TI-RVCO



- **Using a large No. of stage: NxM**
- **Recovering the high-frequency output by combining the inherent multi-phases**

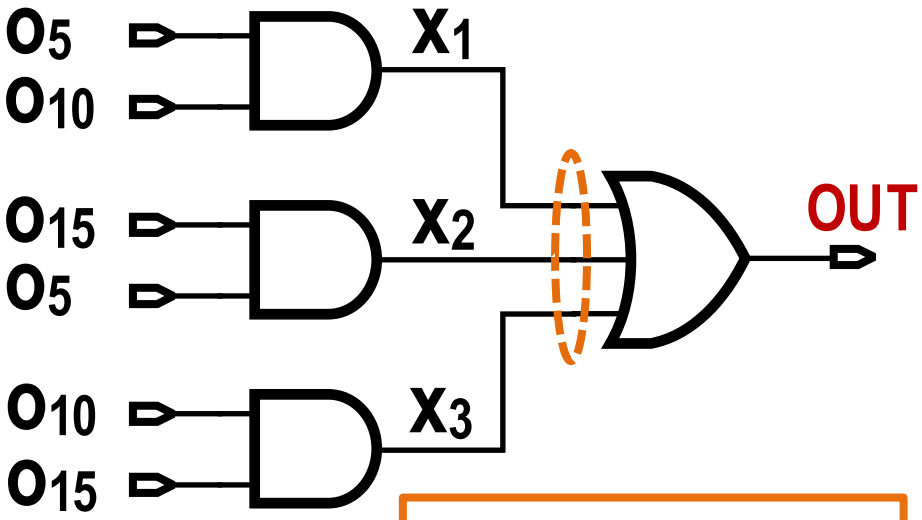
Phase Noise of TI-RVCO

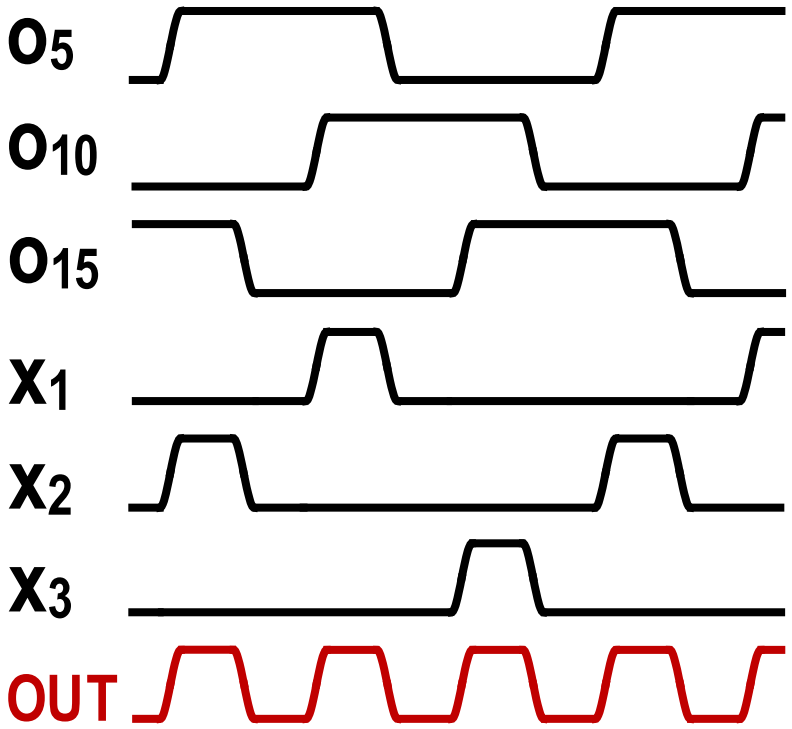


- f_{1/f^3} is reduced by **M** times
- Phase noise at $1/f^2$ region is not degraded

Phase Combiner – Prior Art

[D. Foley et. al., ISSCC'15]





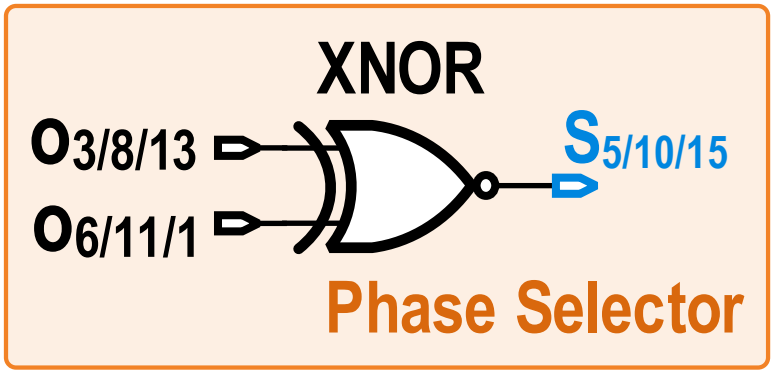
MC Simulation

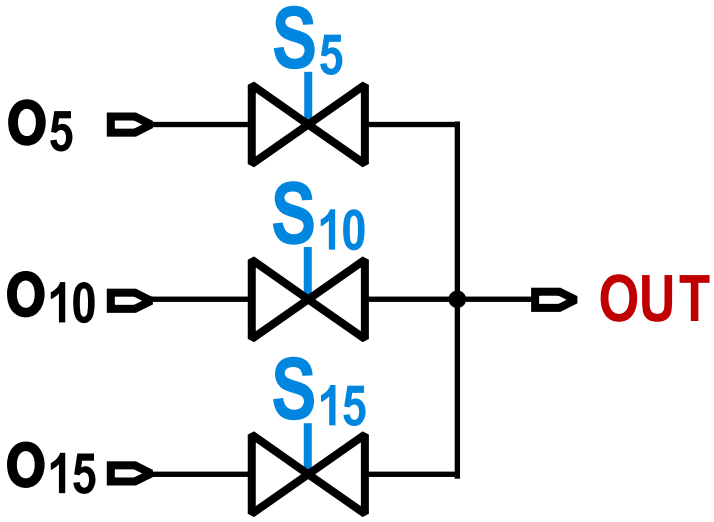
Delay Offset: +4/-6.4ps

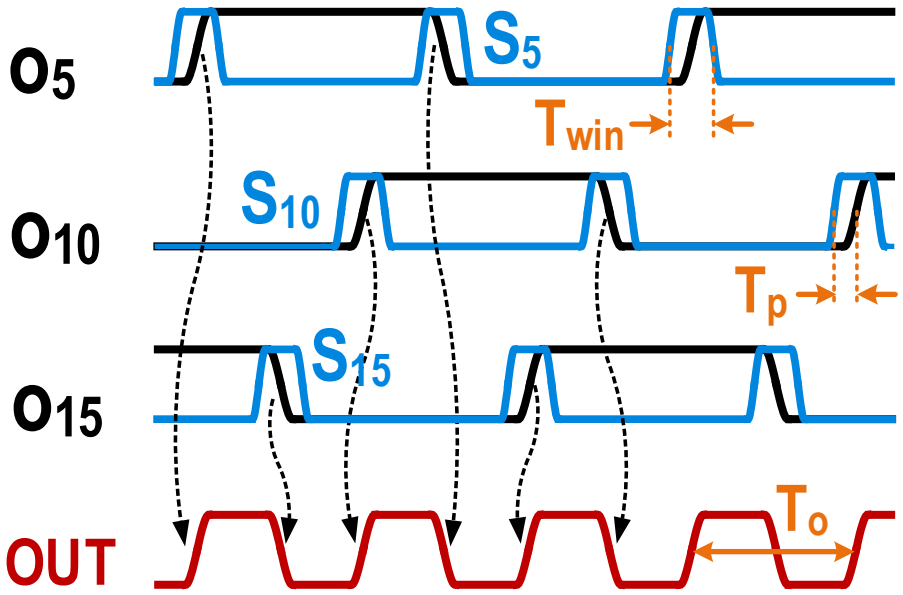
Delay Mismatch: σ=0.39ps

☒ Large delay offset and mismatch in logic-phase combiner

Proposed Time-Window Phase Combiner







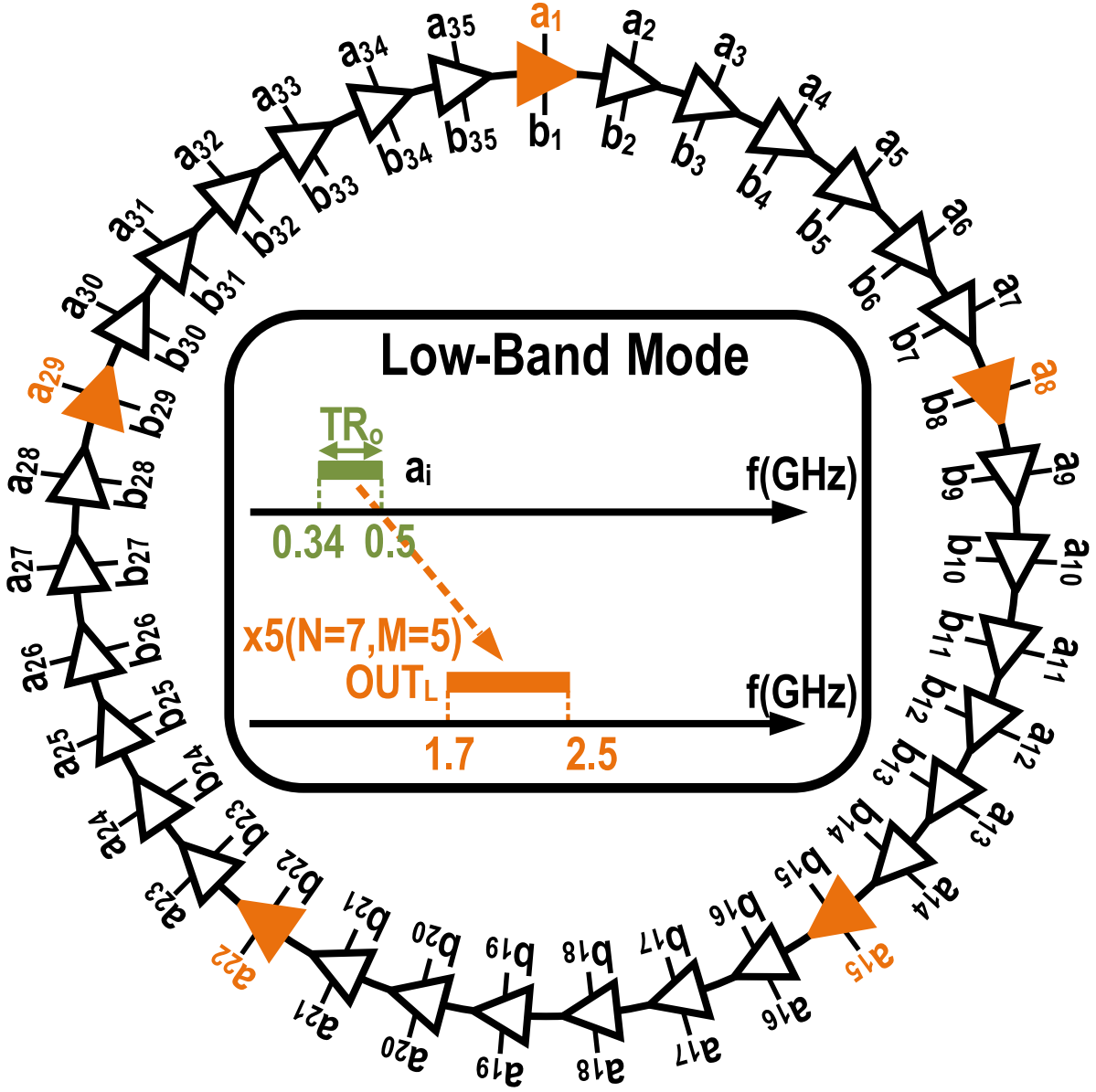
MC Simulation

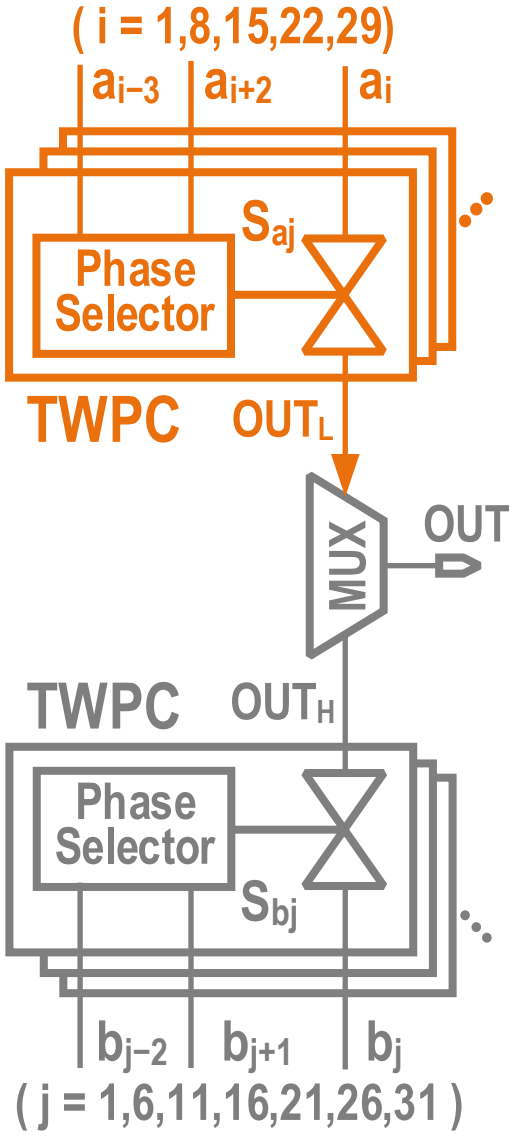
Delay Offset: +10/-8fs

Delay Mismatch: σ=0.12ps

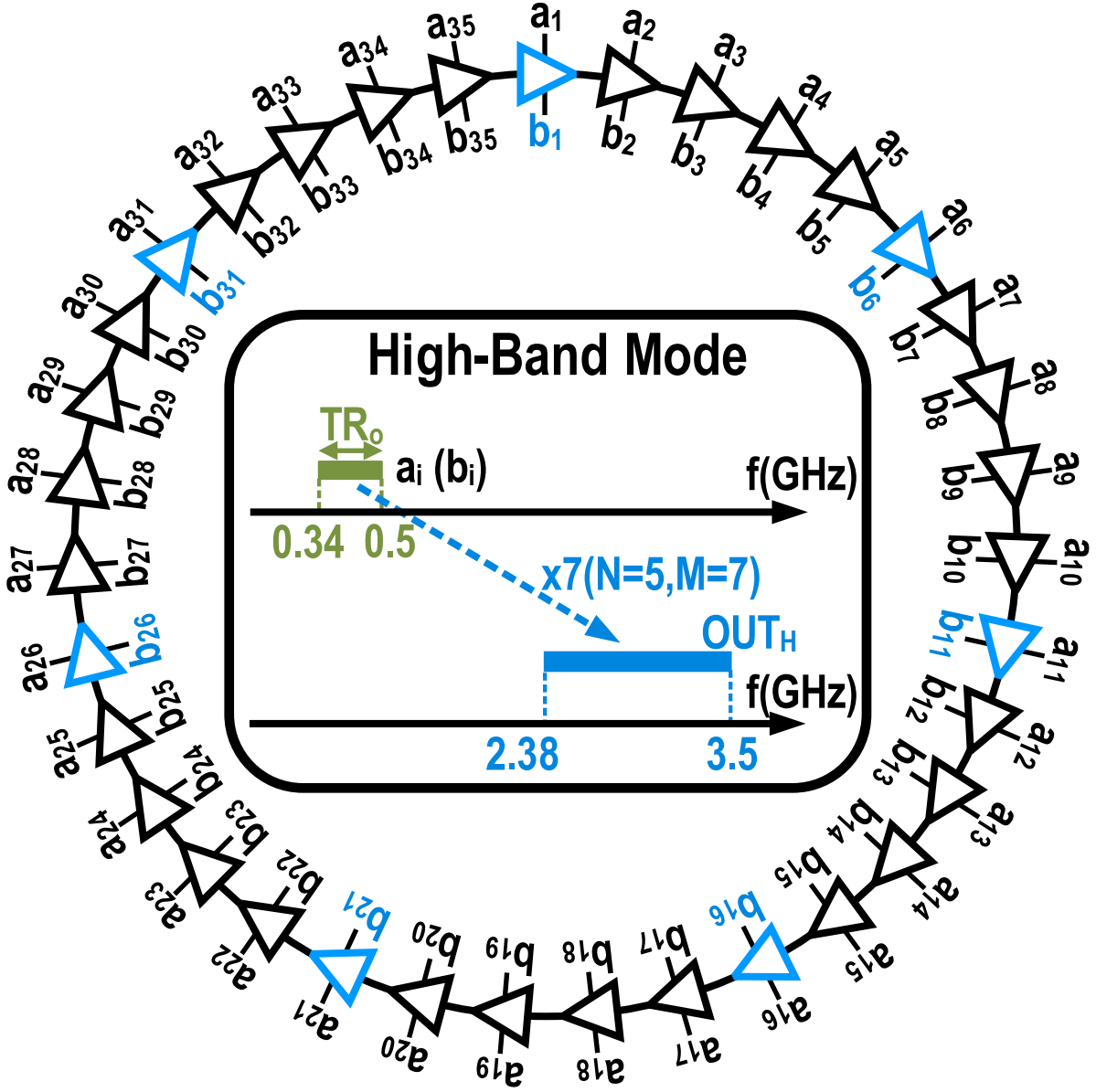
☑ No delay offset and small delay mismatch

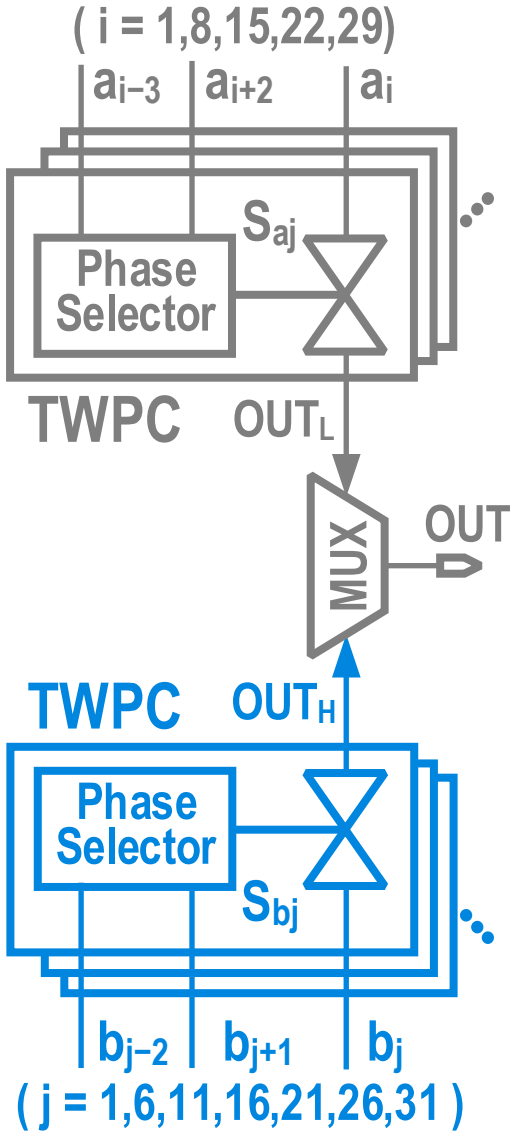
Proposed Dual-Mode TI-RVCO



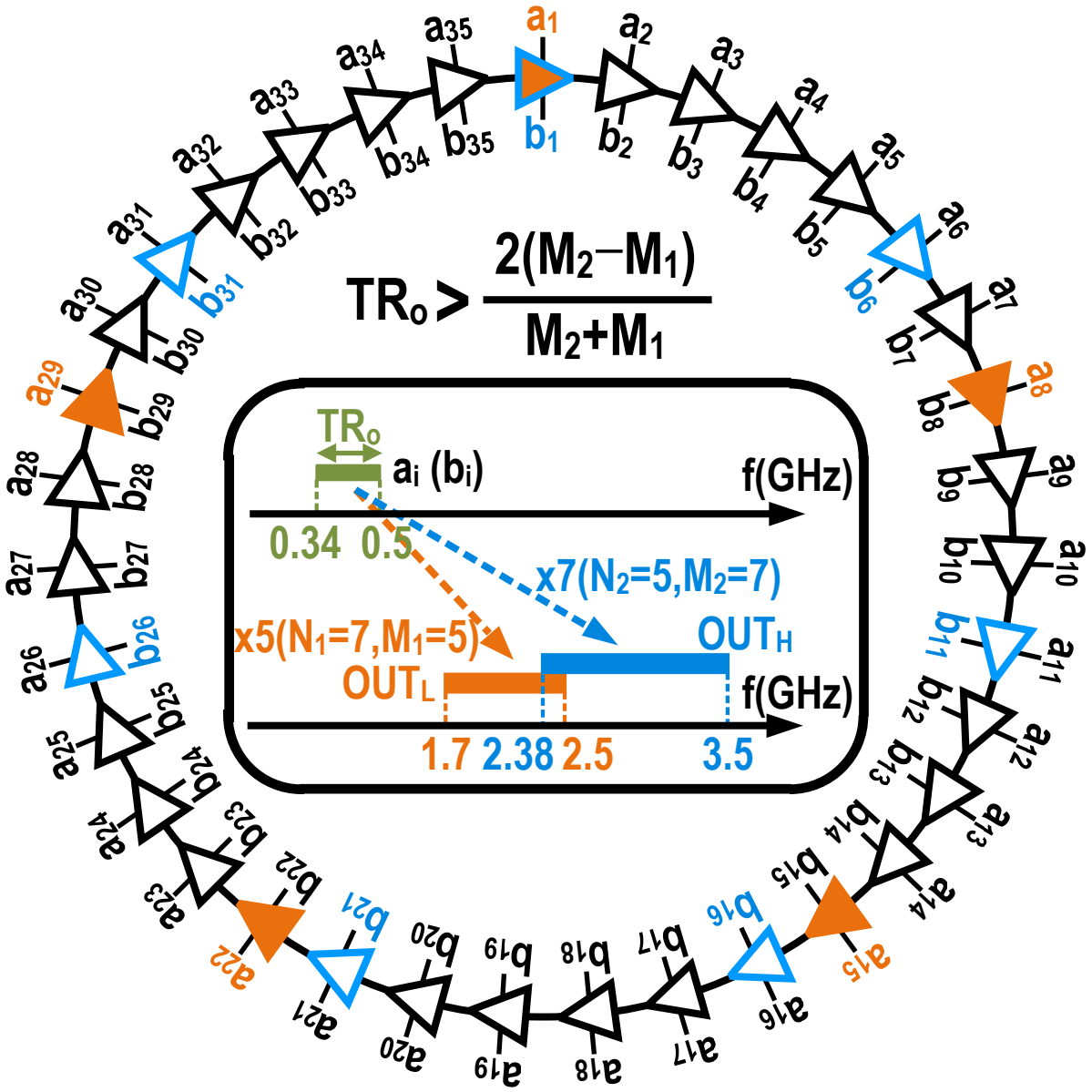


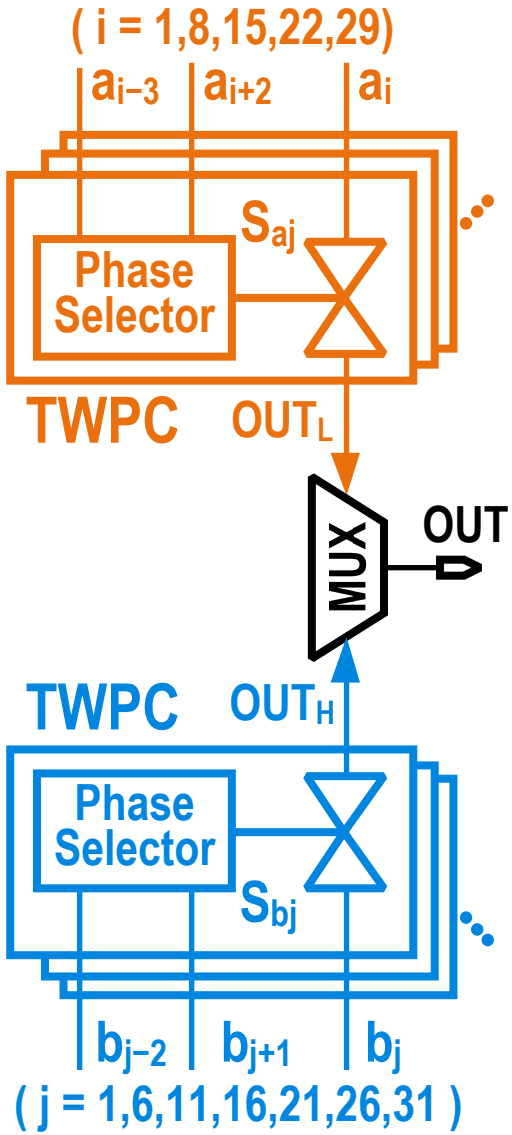
Proposed Dual-Mode TI-RVCO



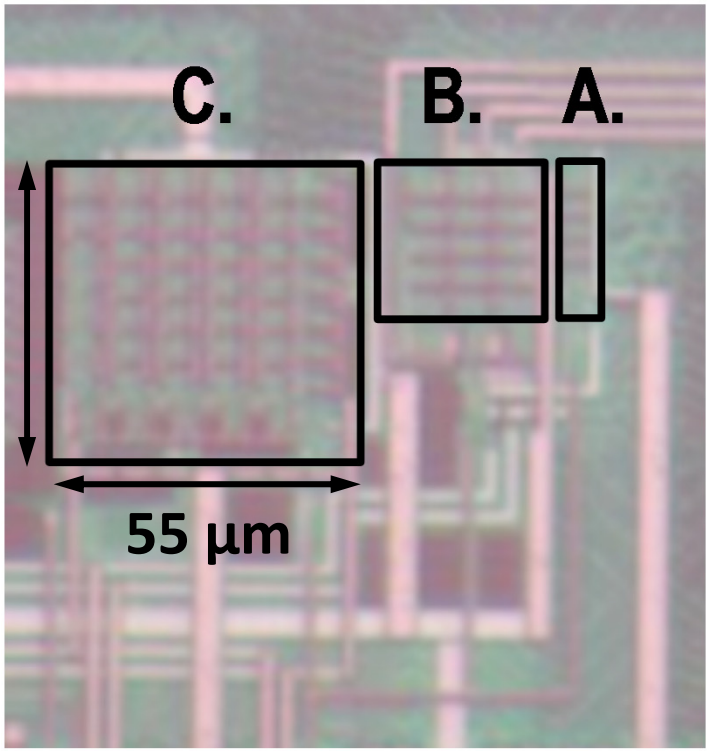


Proposed Dual-Mode TI-RVCO





Chip Photo (65nm CMOS)

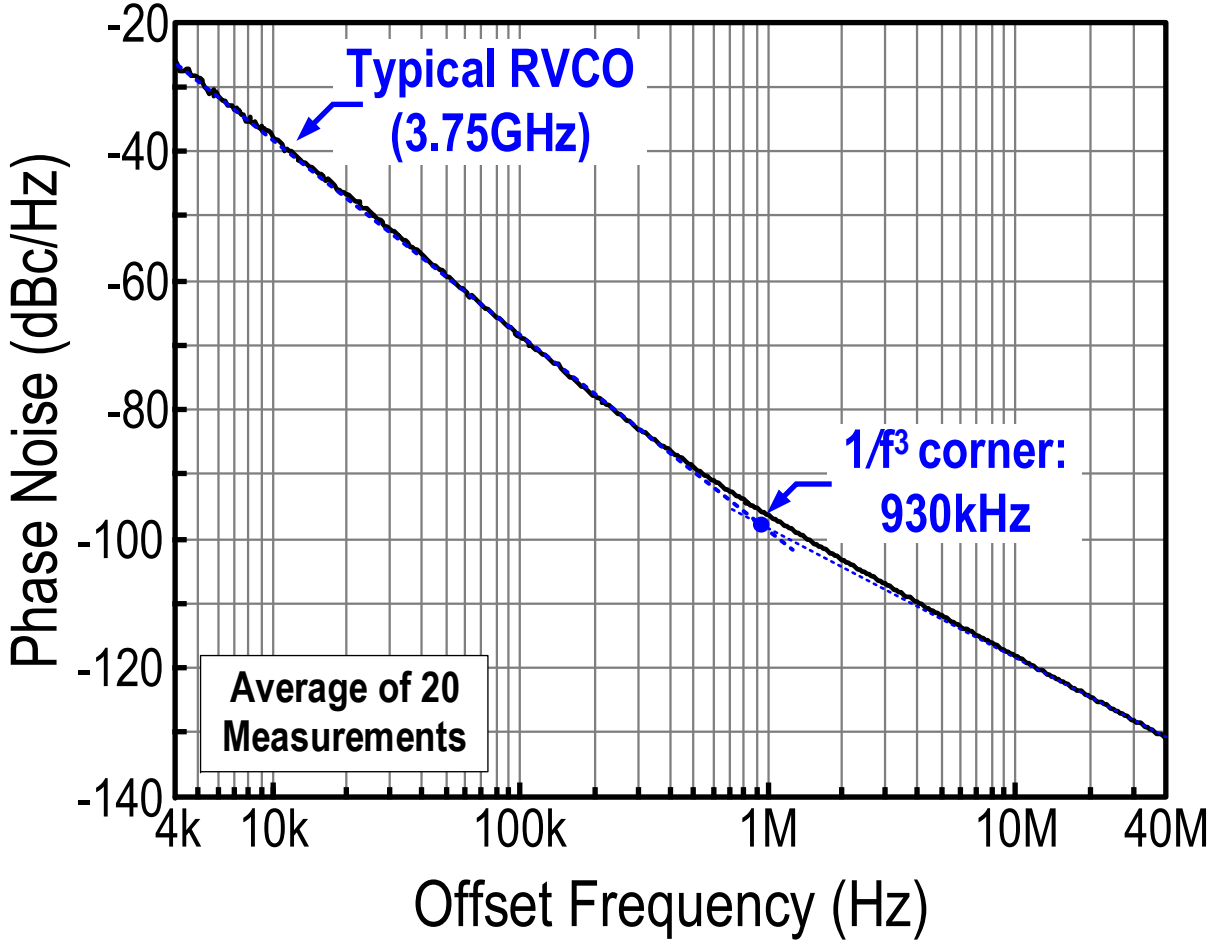


A. 5-Stage RVCO
(0.00024 mm²)

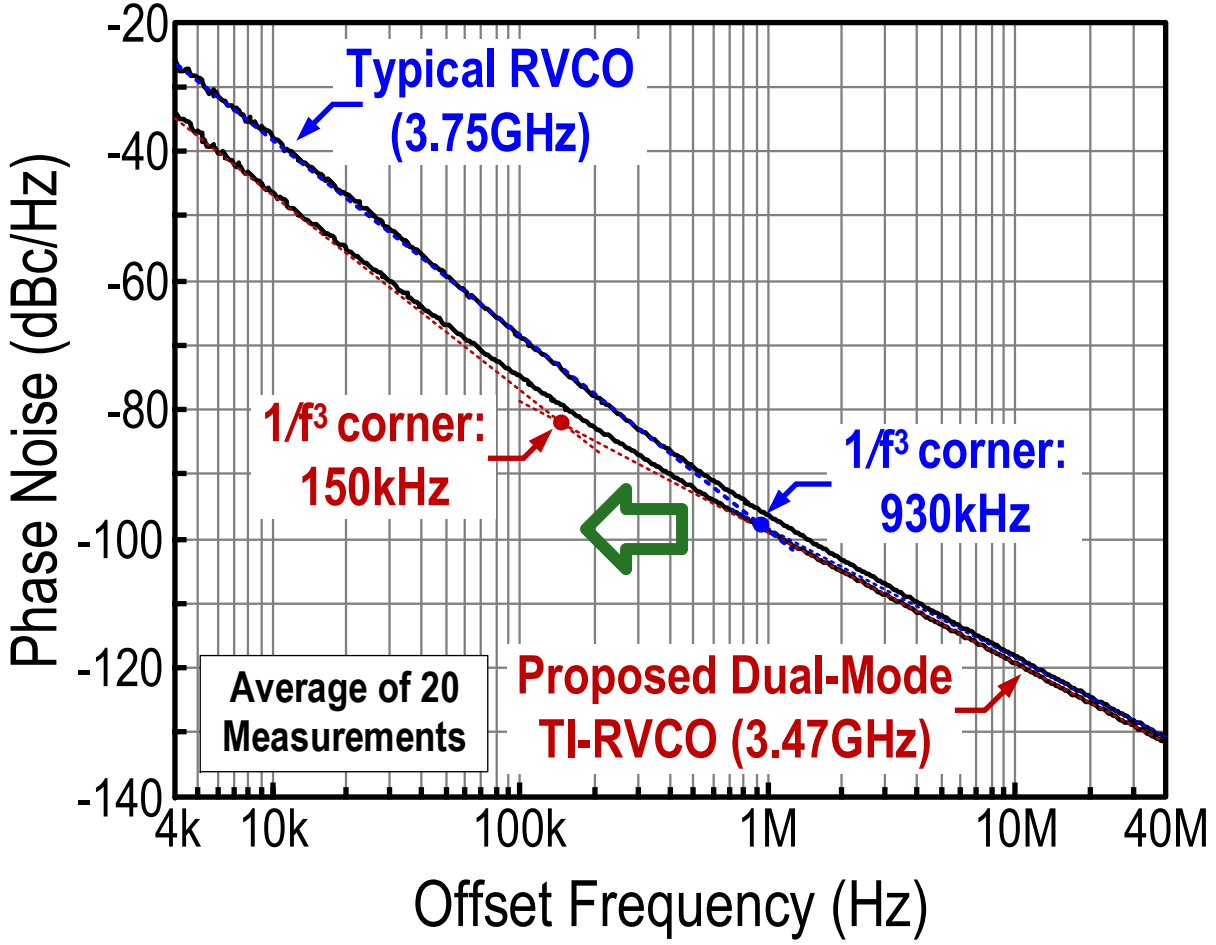
B. 15-Stage TI-RVCO
(0.00086 mm²)

C. 35-Stage Dual-Mode TI-RVCO
(0.003 mm²)

Measured Phase Noise and Tuning Range



Measured Phase Noise and Tuning Range

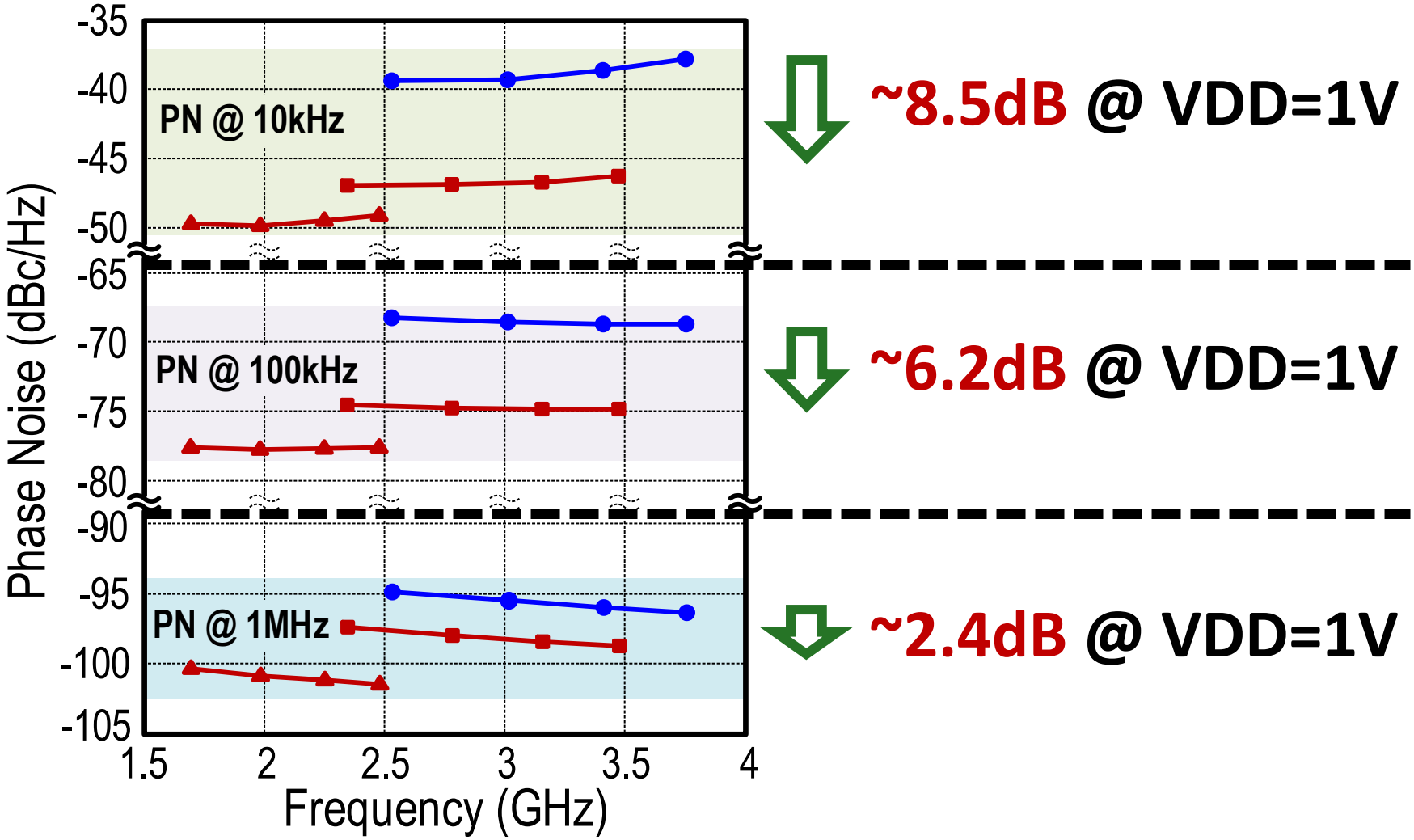


- f_{1/f^3} PN Corner reduced by 6.2x (930kHz → 150kHz)
- Tuning Range increased by 1.45x (V_{DD} from 1 to 0.7 V)

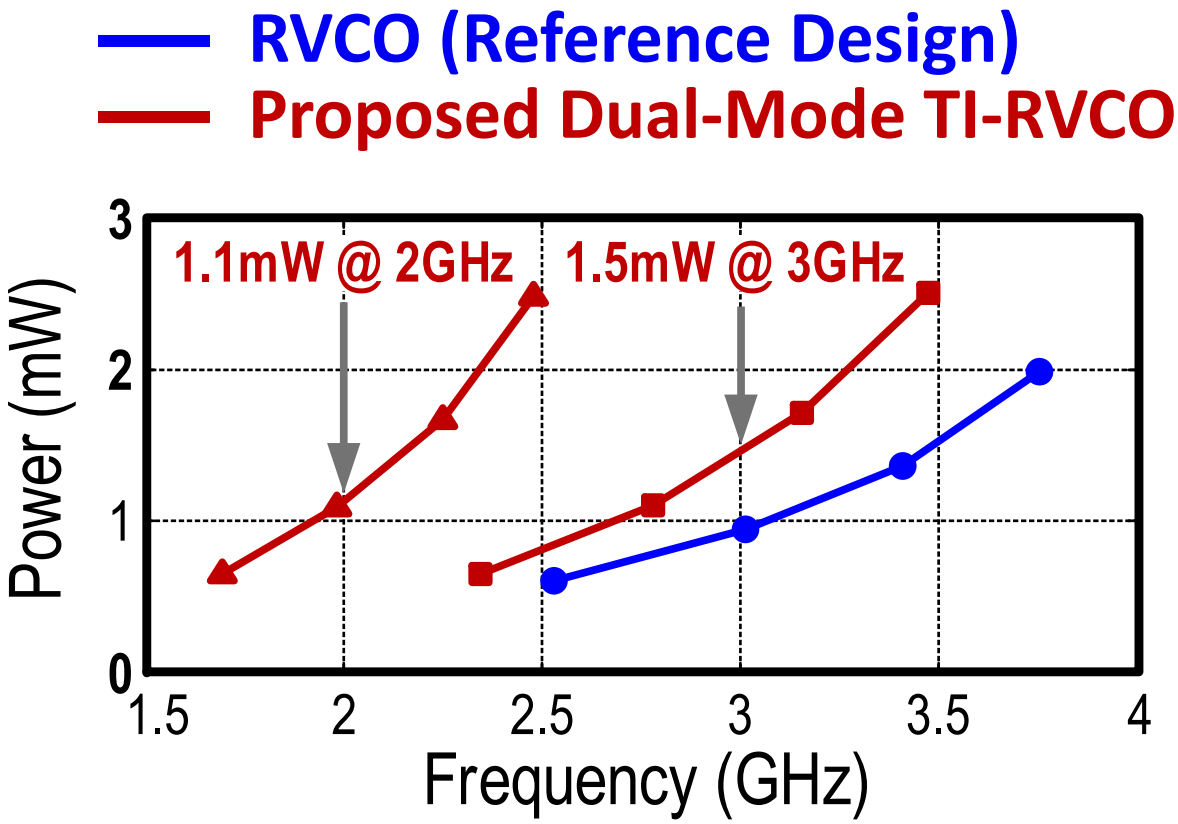
Measured Phase Noise v.s. Frequency

RVCO (Reference Design)

Proposed Dual-Mode TI-RVCO



Measured Power Consumption



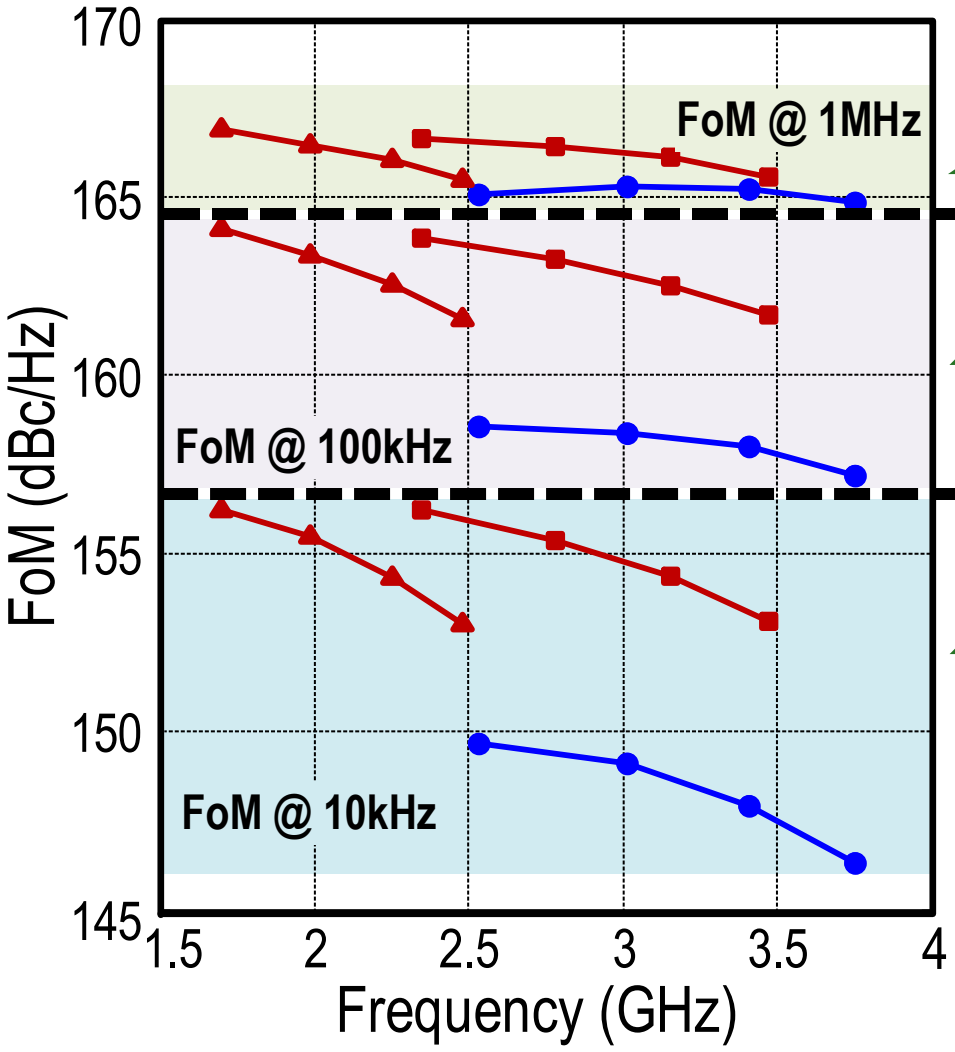
- **Power efficiency @ 3GHz: ~0.5mW/GHz**

(~1.5x of the 5-stage RVCO)

Measured Figure-of-Merit (FoM)

RVCO (Reference Design)

Proposed Dual-Mode TI-RVCO



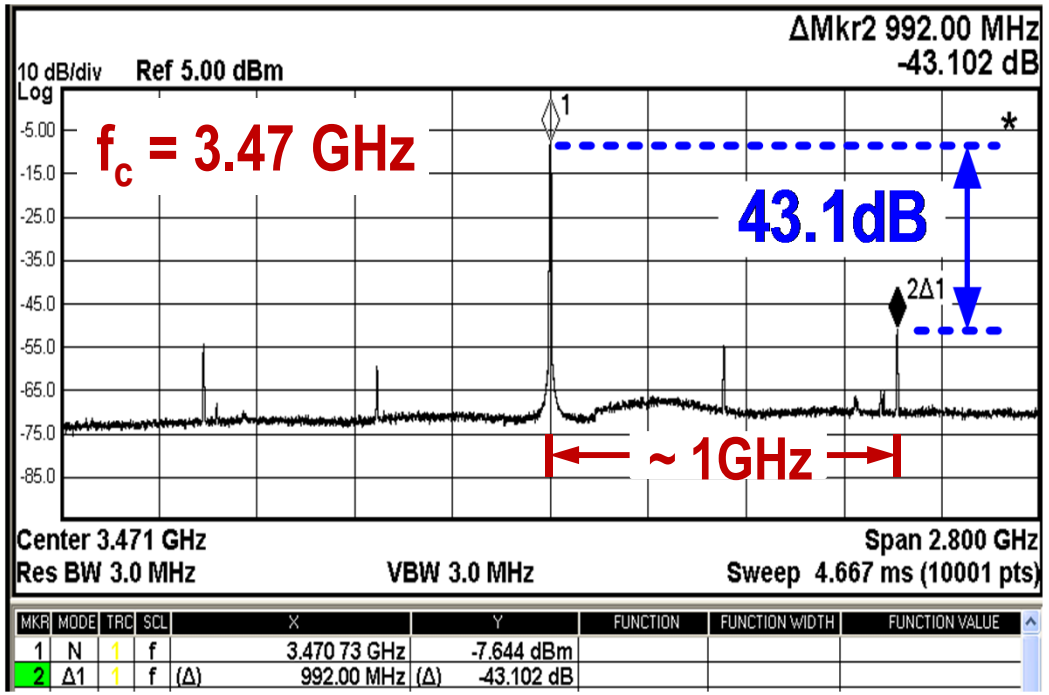
~0.7dB @ VDD=1V

~4.5dB @ VDD=1V

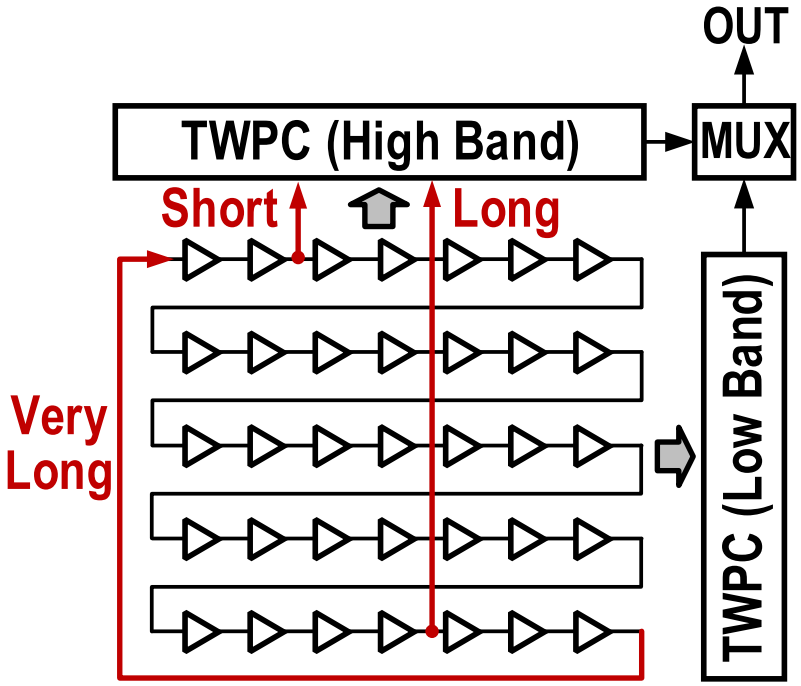
~6.8dB @ VDD=1V

$$FoM = -PN - 10\log(P_{DC}/1mW) + 20\log(f_0/\Delta f)$$

Measured Mismatch Induced Spurs



Layout Plan



- **Output spurs < –43.1dBc**

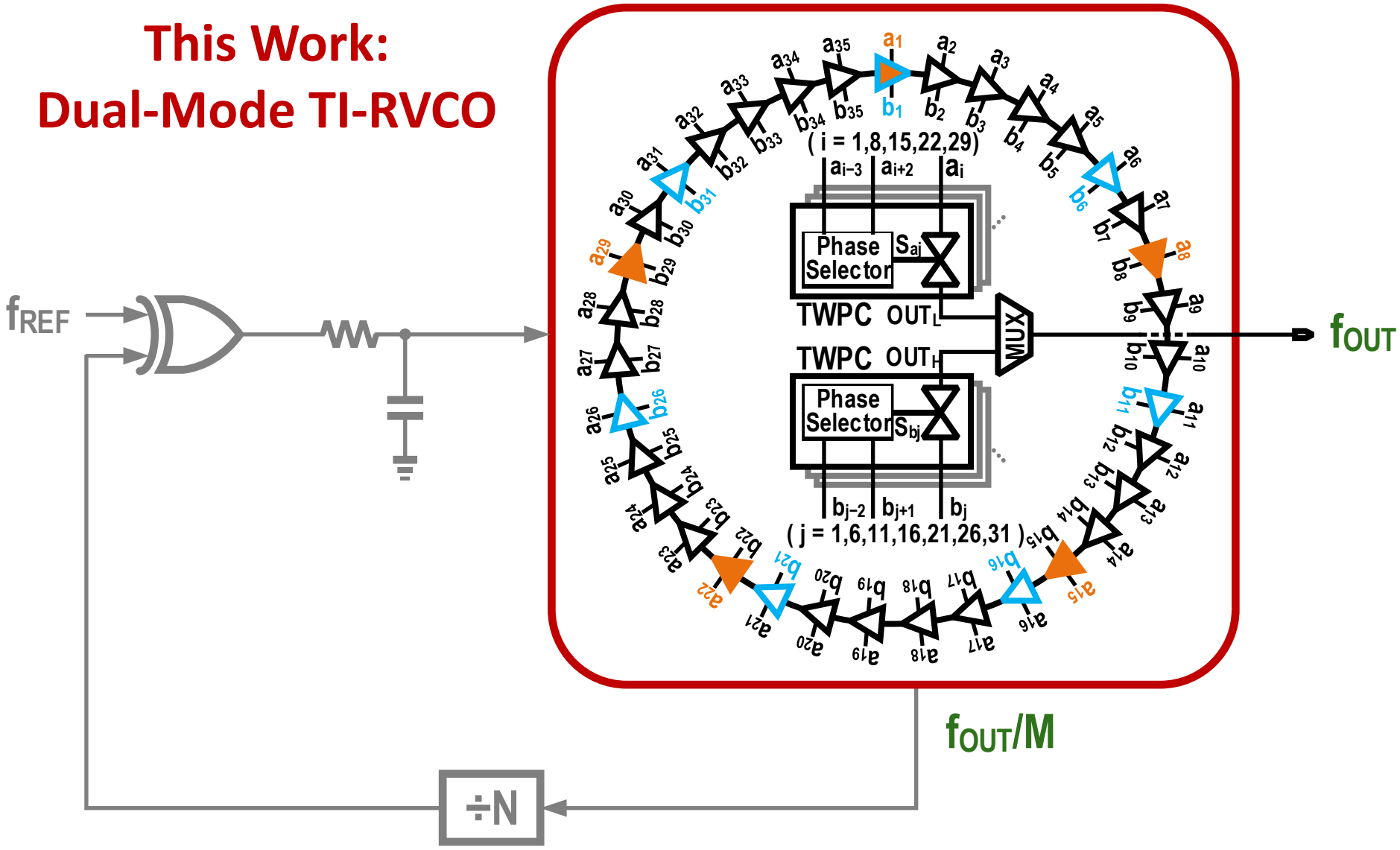
(within frequency offset $f_0 \pm 2f_0/7$)

Comparison with the State-of-the Art

	3 Prototypes Fabricated in This Work				VLSI'14 [6]
Technique	**35-Stage Dual-Mode TI-RVCO**		15-Stage TI-RVCO	Typical 5-Stage RVCO	RVCO + N-Path Filter
Frequency Range (GHz)	1.7 to 3.47 (68.5%)		2.35 to 3.41 (36.8%)	2.53 to 3.75 (38.9%)	0.3 to 1.2 (120%)
Carrier (GHz) @V_{DD}	1.7 @ 0.7V	3.47 @ 1V	3.41 @ 1V	3.75 @ 1V	1.0 @ 1.2V
1/f³ Noise Corner (kHz)	**90**	**150**	340	930	**6000**
Power (mW)	0.65	2.51	2.25	1.99	4.7
PN @ 10kHz (dBc/Hz)	−49.7	−46.3	−43.7	-37.8	N/A
PN @ 100kHz (dBc/Hz)	−77.6	−74.9	−73.6	−68.7	−80
PN @ 1MHz (dBc/Hz)	−100.4	−98.7	−98.9	−96.3	−110
FoM @ 10kHz (dBc/Hz)	**156.2**	**153.1**	150.8	146.3	N/A
FoM @ 100kHz (dBc/Hz)	**164.1**	**161.7**	160.7	157.2	**153.3**
FoM @ 1MHz (dBc/Hz)	**166.9**	**165.6**	166.0	164.8	**163.3**
Core Area (mm²)	**0.003**		0.00086	0.00024	**0.015**
CMOS Technology	65nm		65nm	65nm	65nm

Conclusion

This Work:
Dual-Mode TI-RVCO



Acknowledgments

- **Multi-Year Research Grant of University of Macau**
- **Macao Science and Technology Development Fund (FDCT)**

A Mixed-Mode Injection Frequency-Locked Loop for Self-Calibration of Injection Locking Range and Phase Noise in 0.13μm CMOS

Dongseok Shin, Sanjay Raman, Kwang-Jin Koh

Multifunctional Integrated Circuits & Systems Group

Virginia Tech, Blacksburg, VA

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Outline

- Motivation
- Previous Frequency Calibration Circuit for ILO
- Proposed Injection Frequency-Locked Loop (IFLL)
- Circuit Implementation
- Measurement Results
- Conclusion

Motivation

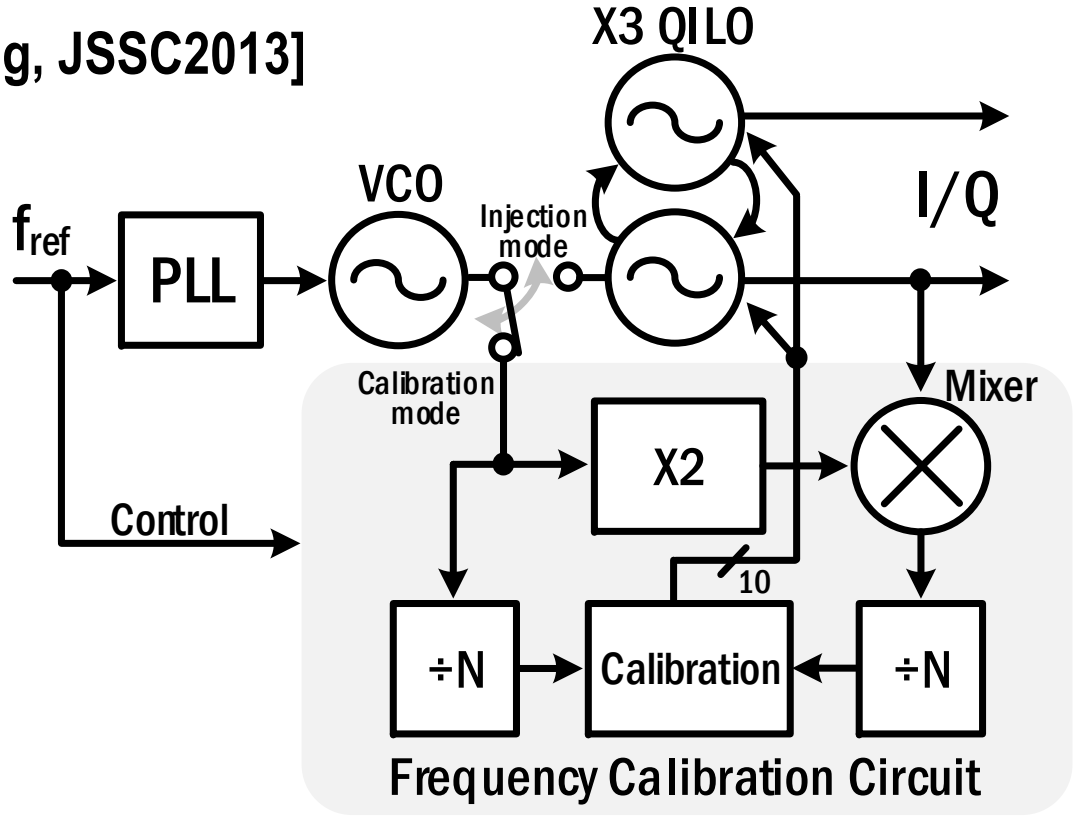
- Subharmonic injection-locked oscillator (ILO) at mm-Wave
  - ☺ Good phase noise performance
  - ☺ No mm-wave frequency divider in frequency synthesizer
  - ☺ Low power consumption of LO distribution
  - ☹ Narrow locking range (typically < 3%)
  - ☹ Phase noise degradation at the edge of locking range

    → reduce effective locking range

- To solve the problems, a frequency calibration circuit is required.

Prior Art: Frequency Calibration for QILO

[Deng, JSSC2013]



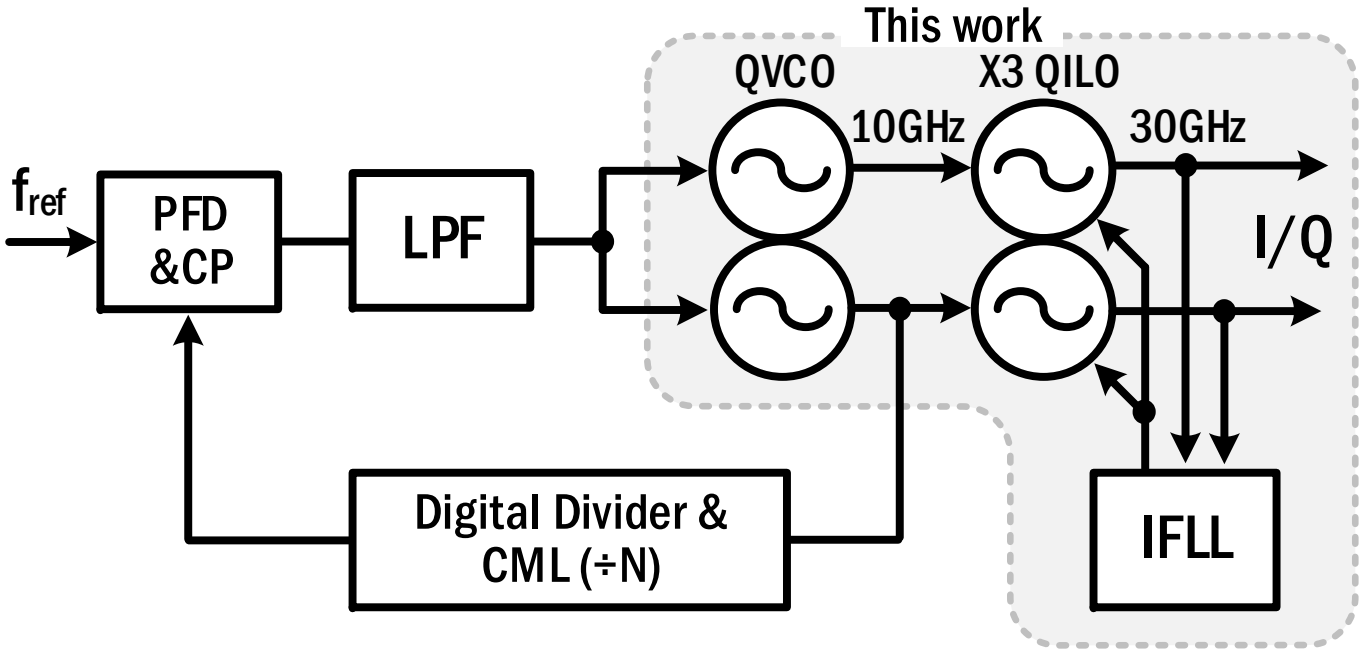
☺ Accurate freq. calibration → Minimum I/Q error, no PN degradation

☹ Multi-frequency domain approach → frequency up/dn

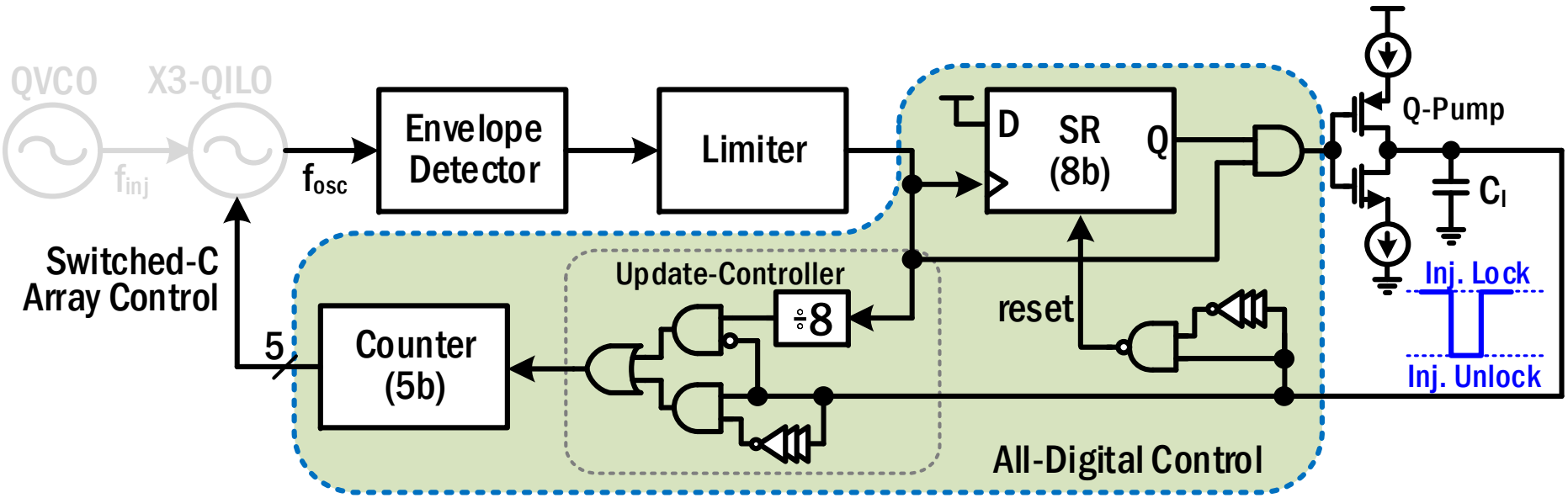
☹ Hardware complexity, large P_{diss} (~65mW), long locking time (< 42.7us), and external control

mm-Wave PLL with IFLL

- **QVCO + QILO + IFLL**
  - QVCO: Improve locking range and phase accuracy of QILO
  - QILO: 3rd-harmonic injection locking w/ 5bit switched-C array
  - IFLL: Autonomous calibration of injection locking range and PN



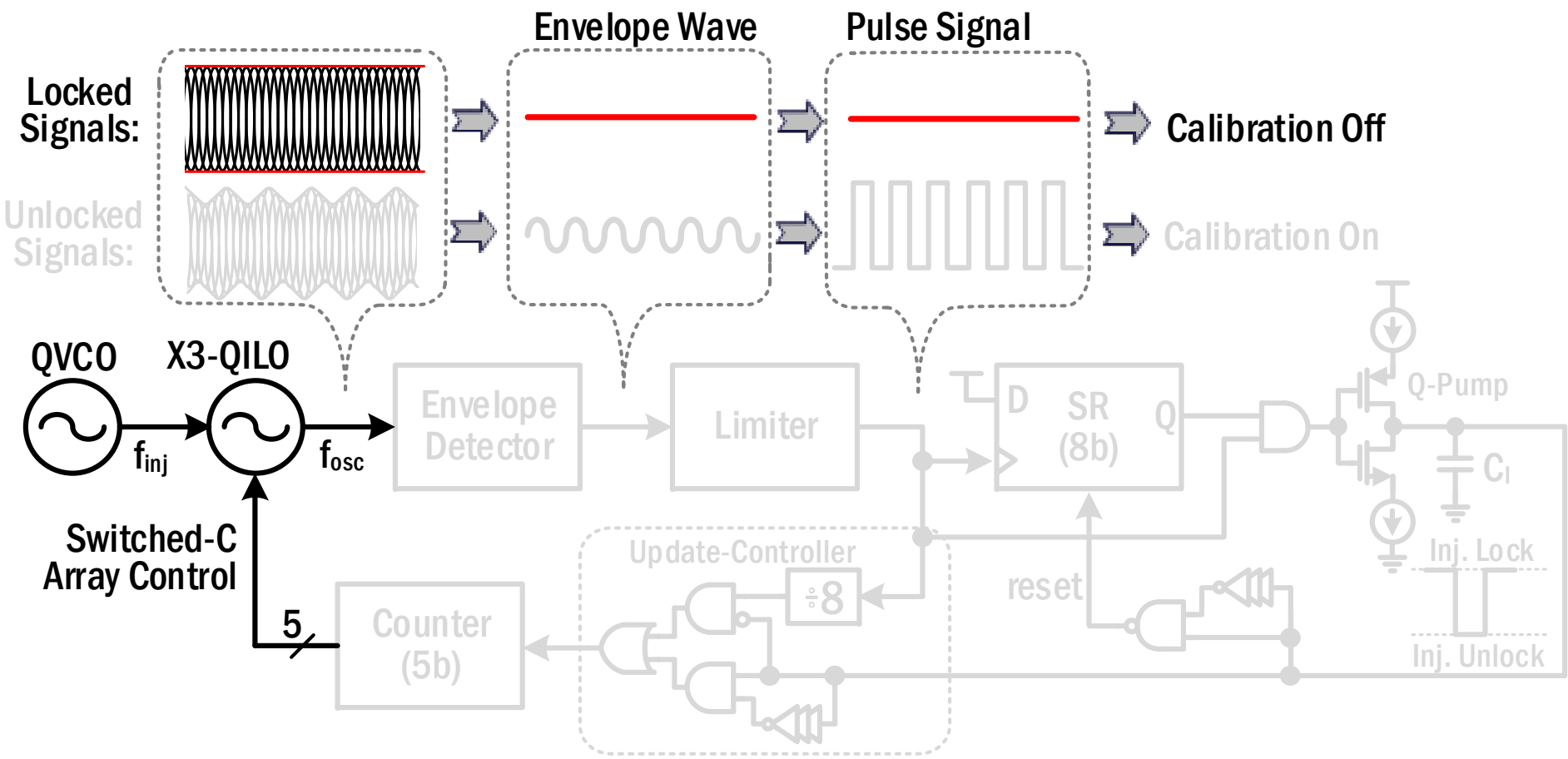
Proposed Injection Frequency-Locked Loop



- **Design objectives of IFLL**
  - Envelope detection → injection-locking detection [T-MTT2009, JSSC2011]
  - Autonomous feedback calibration → no external control
  - Envelope-to-pulse conversion
  - All-digital feedback control

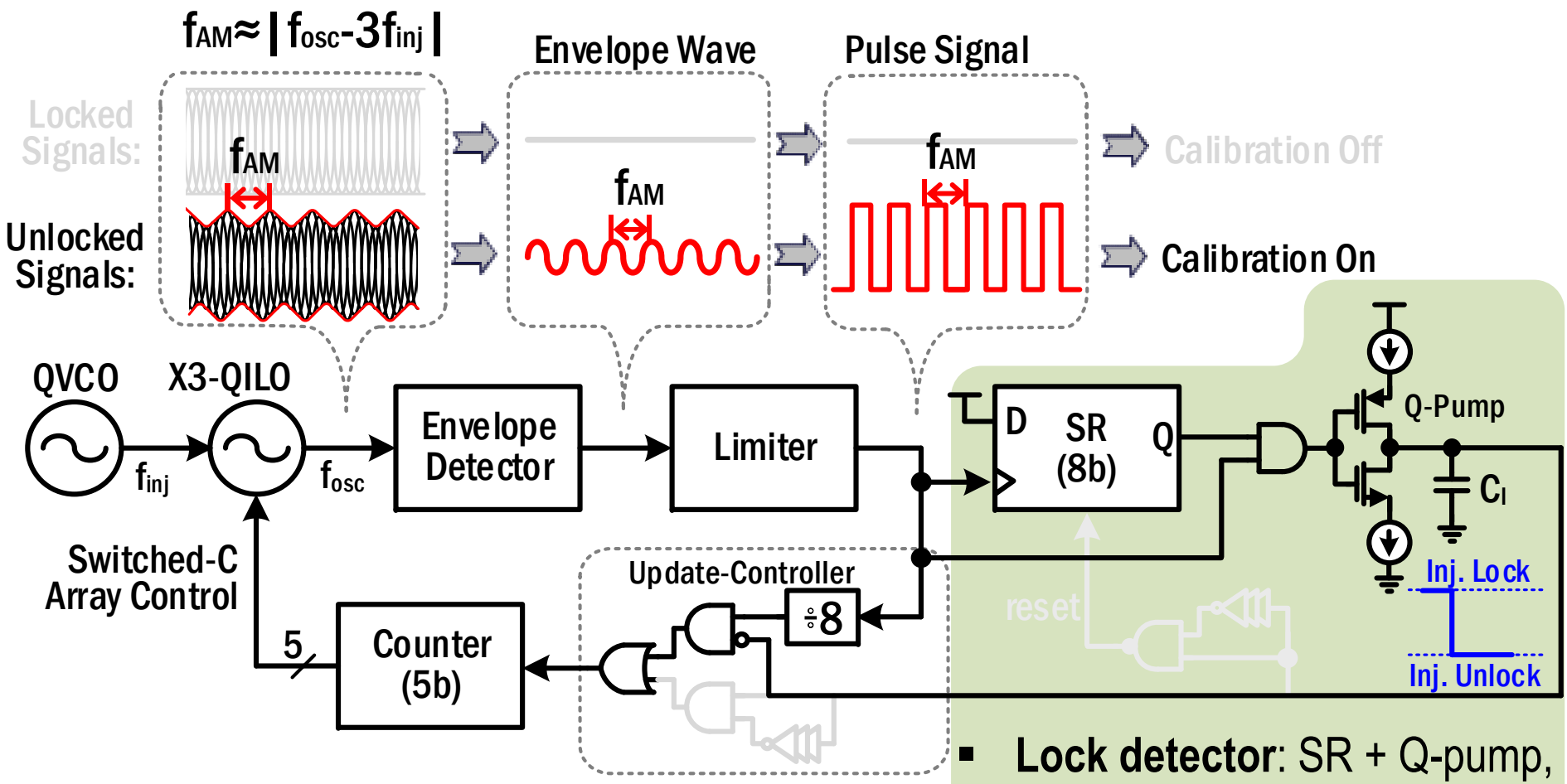
  → fast locking time
  - PN calibration → avoid PN degradation

① Locked Condition



- Injection-locked signals: No envelope wave → Calibration off

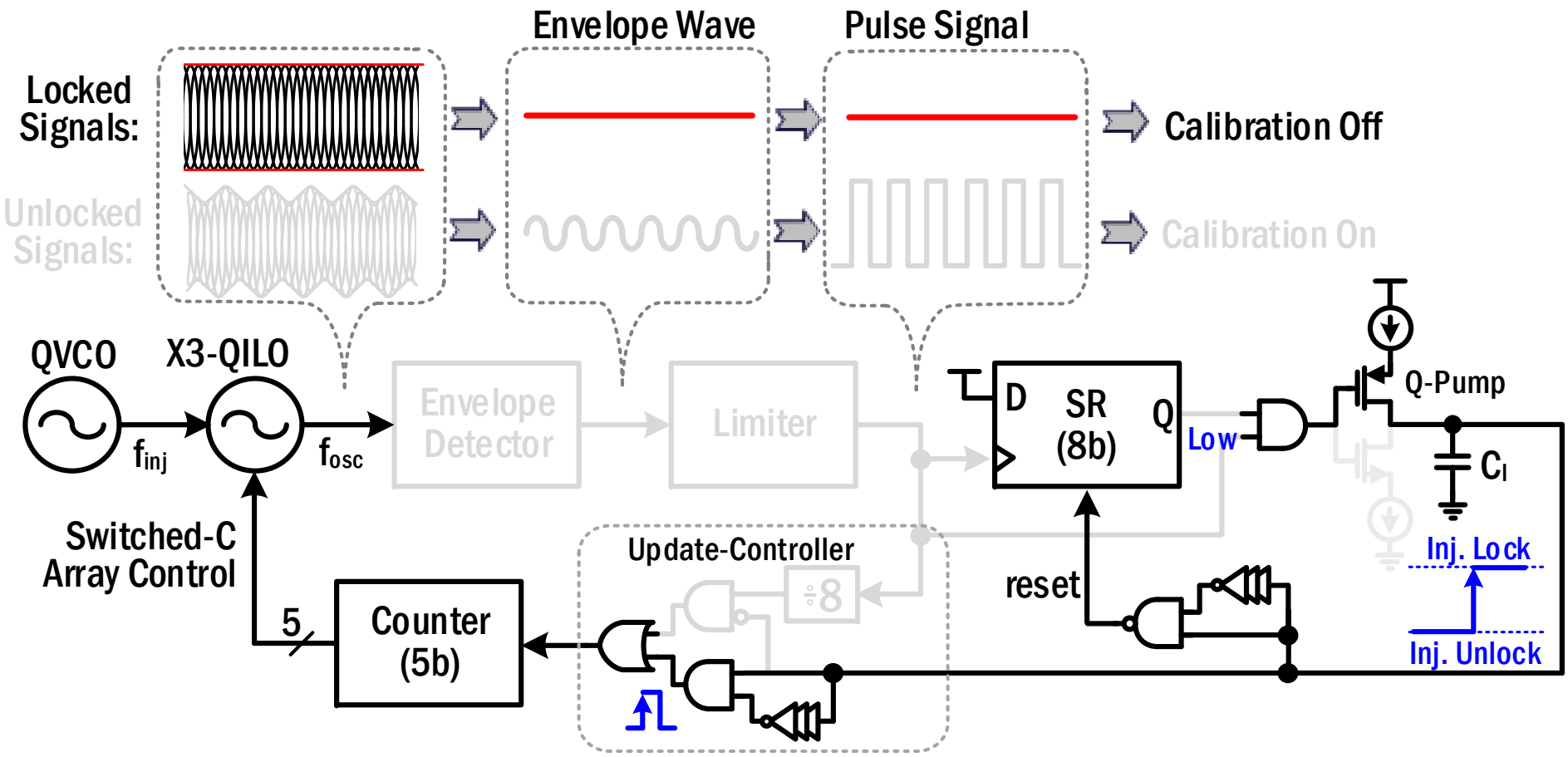
② Unlocked Condition: Frequency Calibration



- Why ÷8? → to ignore 3 or 4 irregular pulses from limiter when codes are changed.

- **Lock detector**: SR + Q-pump, to control update-controller

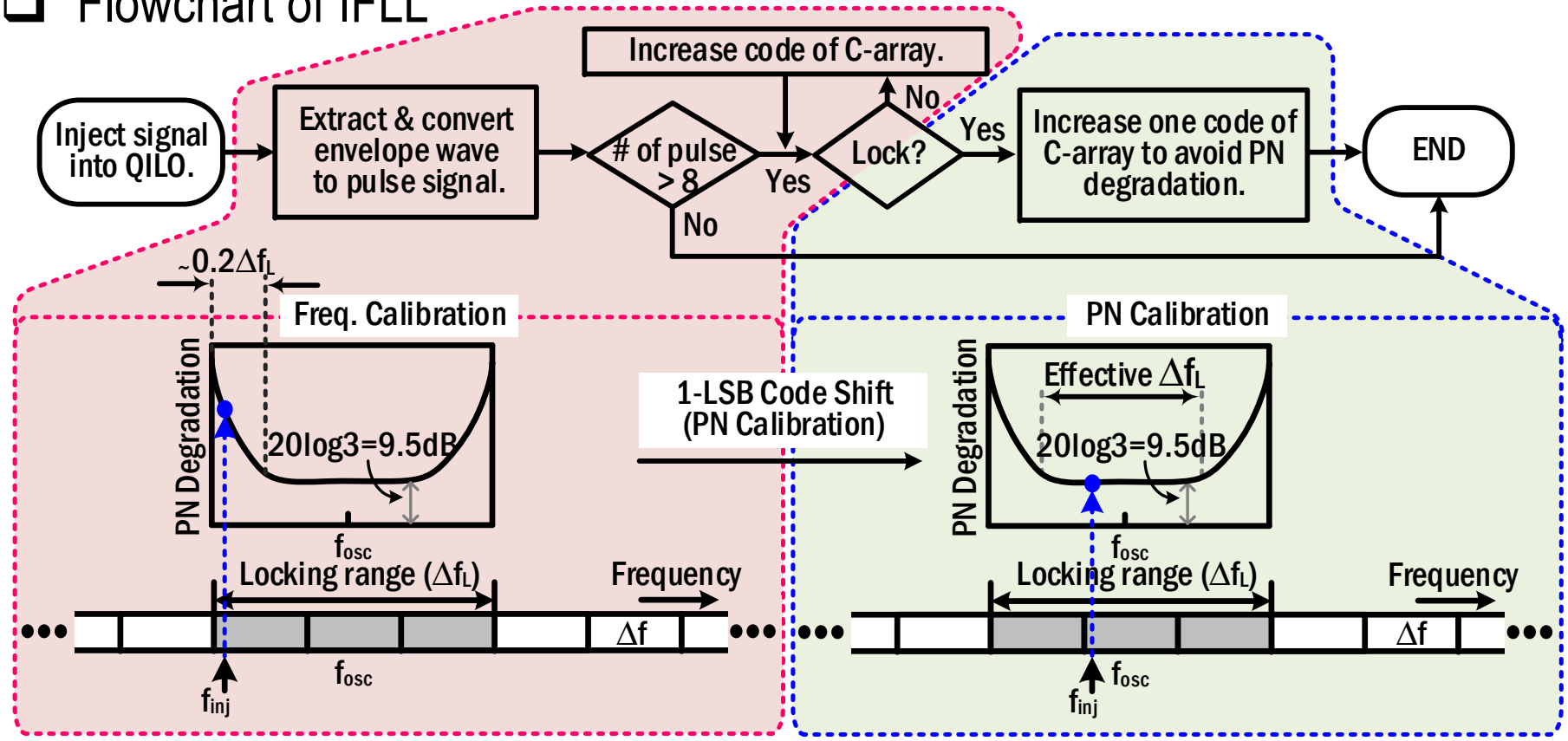
③ After Locking: Phase Noise Calibration



- After calibration, lock signal → Push 1 LSB of the counter
  → Phase noise calibration and SR reset

Phase Noise Calibration Details

- Flowchart of IFLL

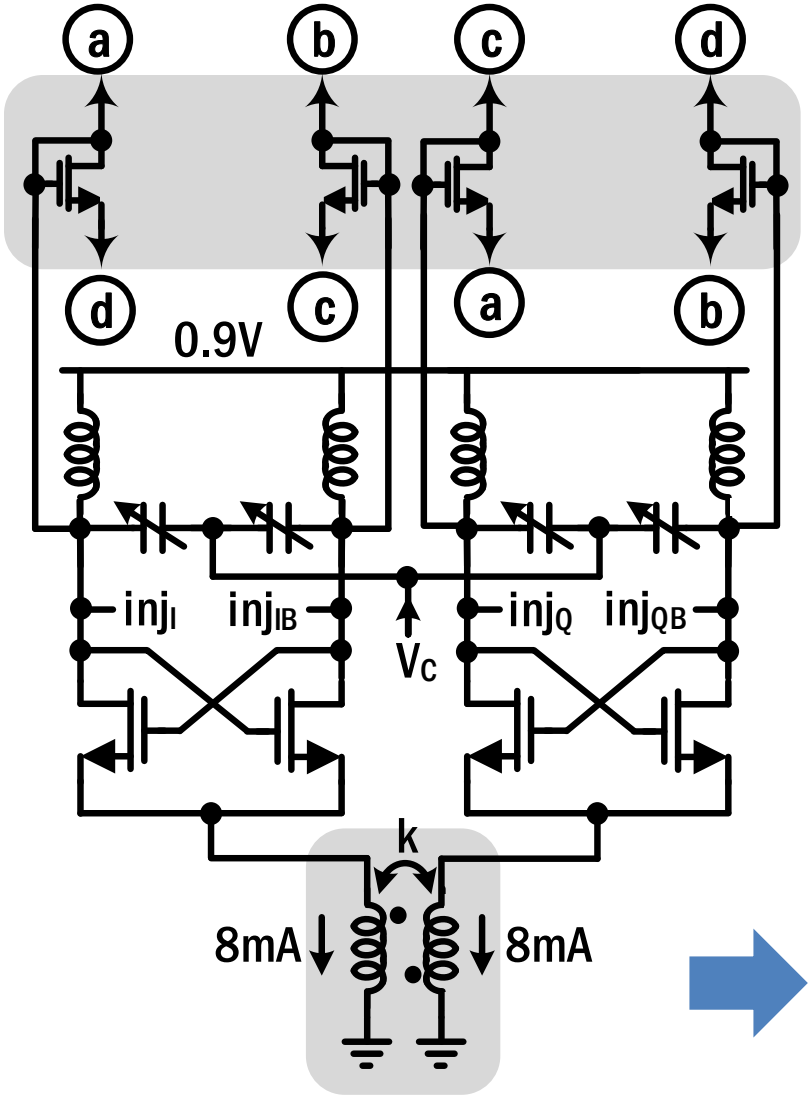


- Assume PN degrades at 20% of Δf_L on each edge.
- Requirement on frequency resolution (Δf):

$$f_{AM,MIN} + 0.2\Delta f_L \le \Delta f \le \tfrac{1}{2}(f_{AM,MIN} + 0.8\Delta f_L)$$

- $f_{AM,MIN}$: Minimum detectable frequency of ED and limiter

QVCO for Quadrature Injection Signals



In-phase injection-coupling
[Yi, JSSC2014]

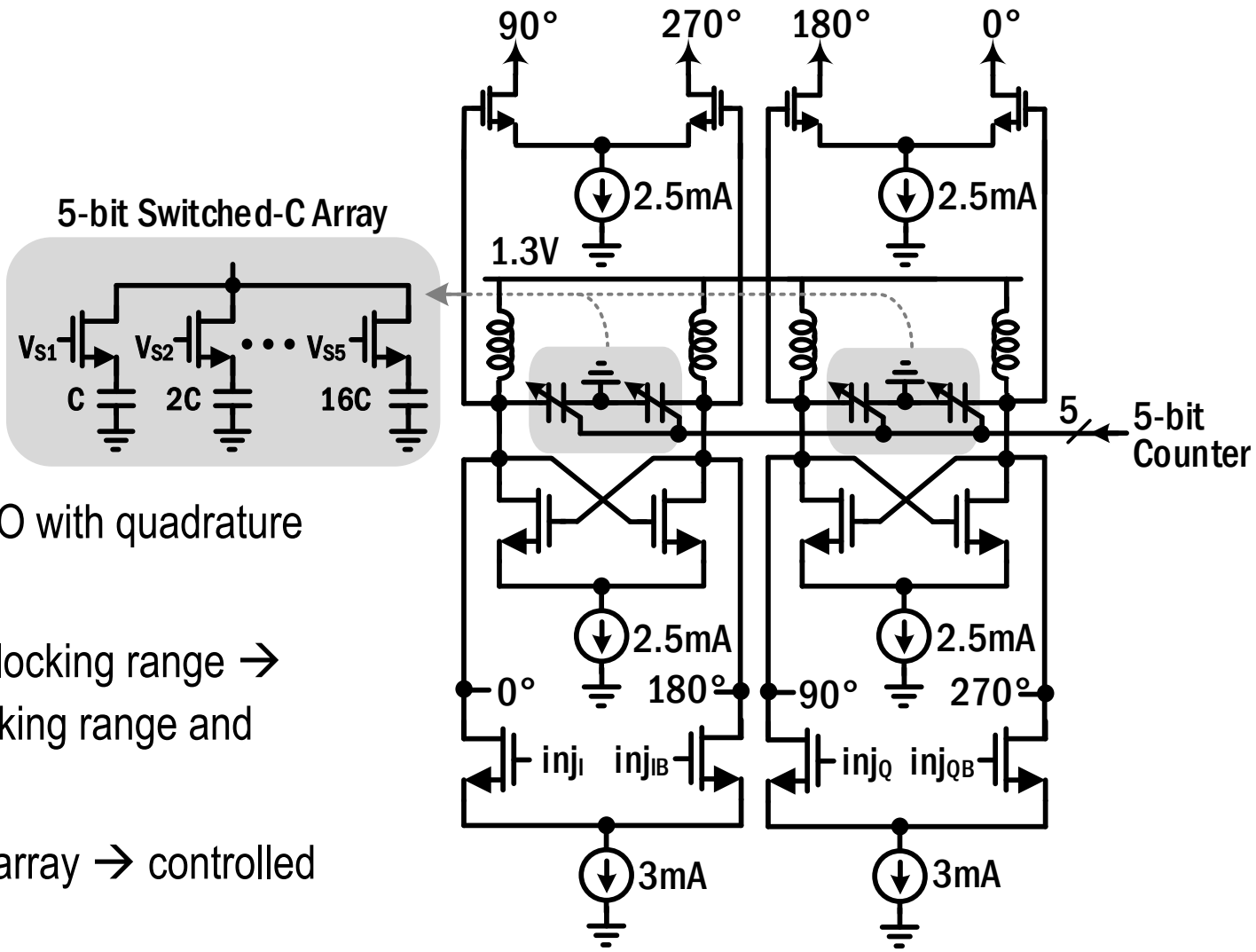
I/Q directivity & Less I/Q error

+

Low phase noise

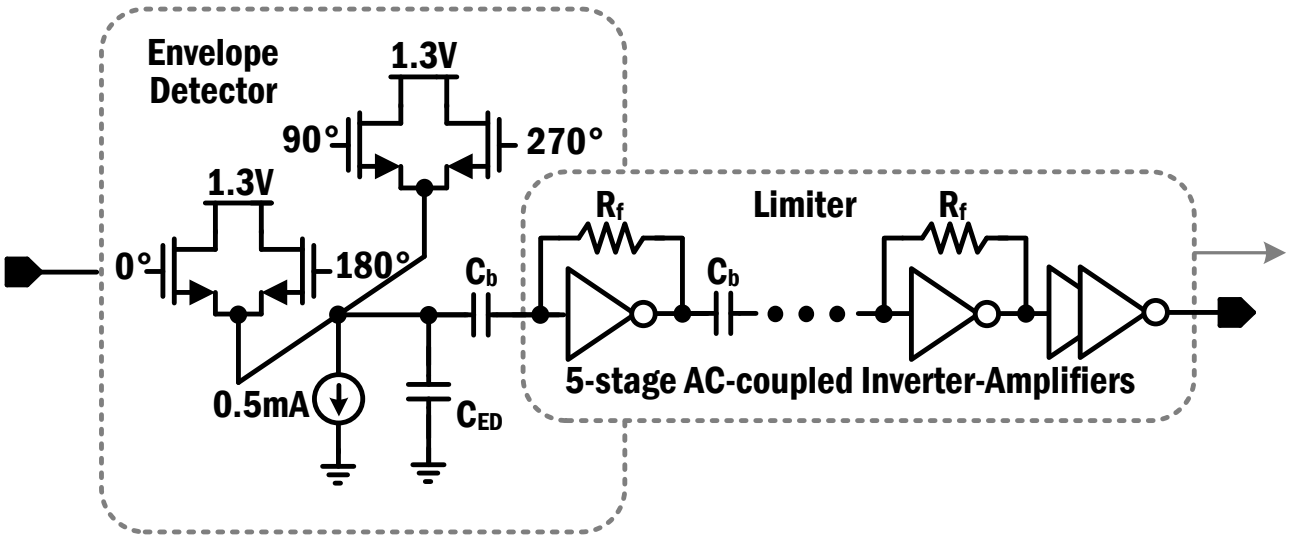
Super-harmonic coupling
[Gierkink, JSSC2003]

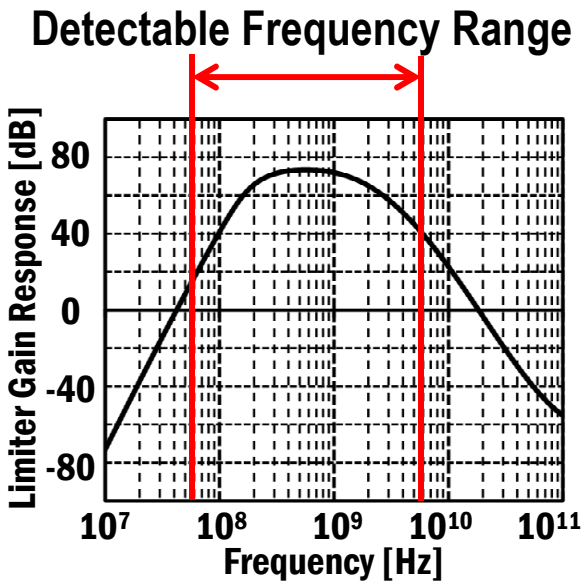
QILO w/ Current-Injection Cross-Coupling



- 3rd-harmonic ILO with quadrature coupling
- Typically < 3% locking range → tradeoff b/w locking range and output swing
- 5b switched-C array → controlled by IFLL

Envelope Detector with Limiter

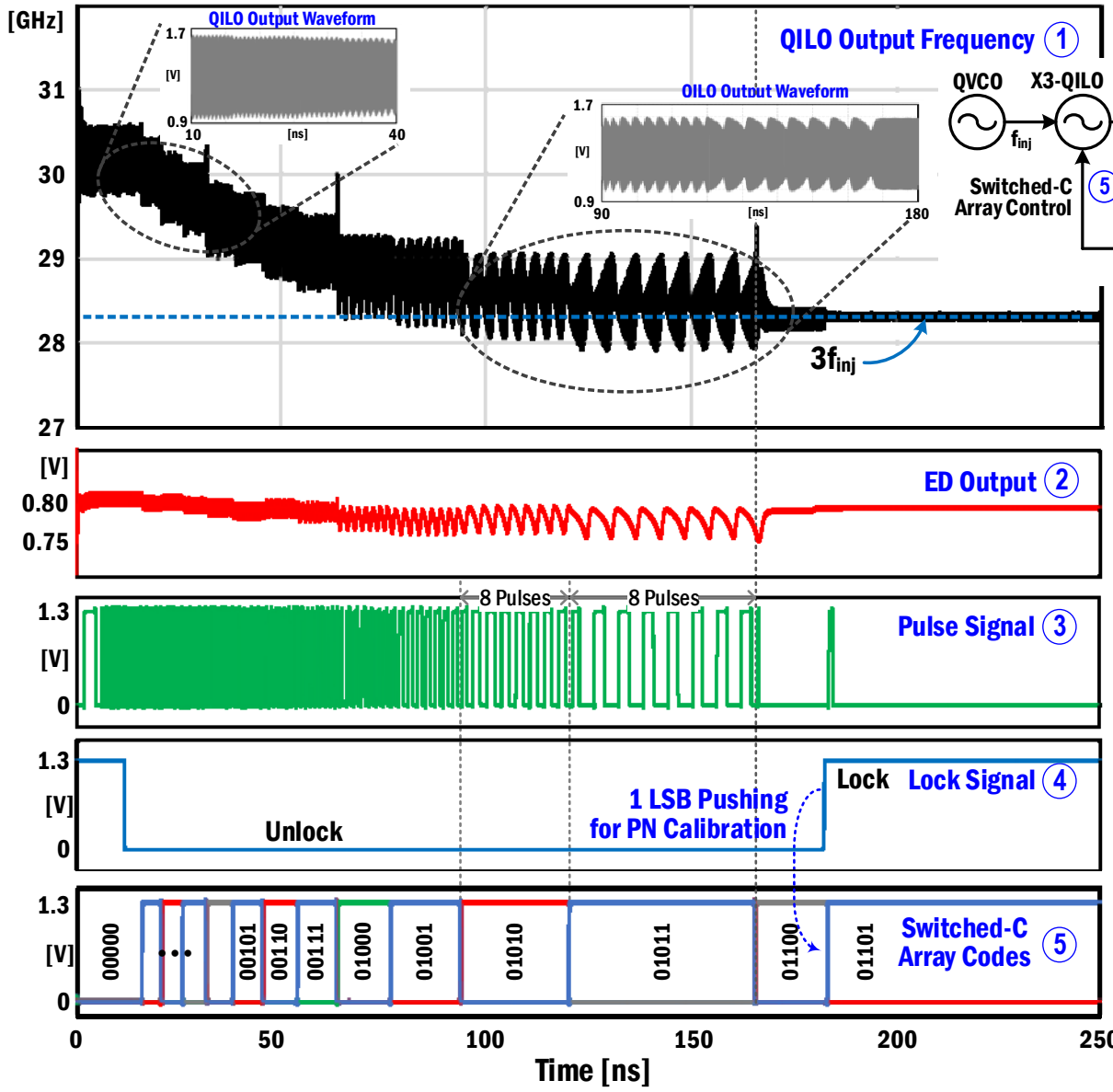


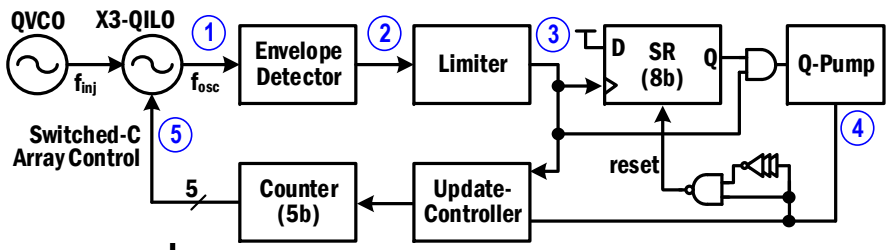


- Envelope detector (ED): source follower and load capacitor (C_{ED})
- Limiter: 5-stage AC-coupled feedback-inverter amplifiers to generate pulse signal from envelope wave.

- Low band (<~ 60MHz) filtered out to prevent ED from detecting quasi-lock.
- High band determines maximum detectable frequency.

Transient Simulation Results

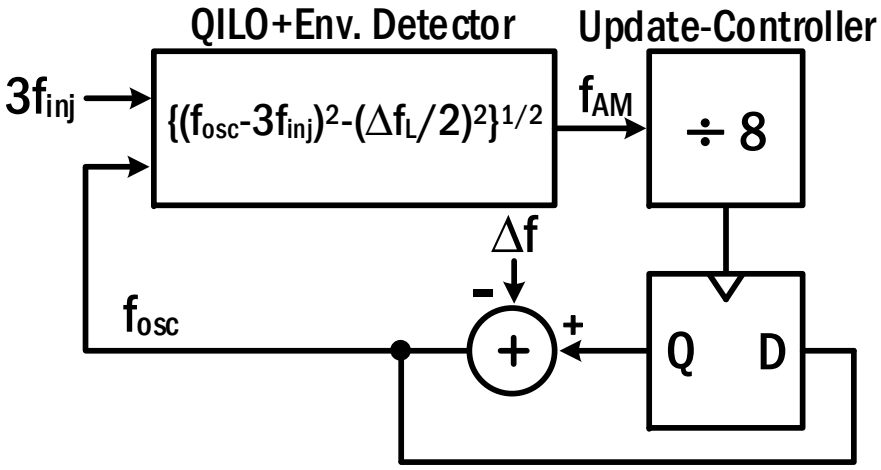




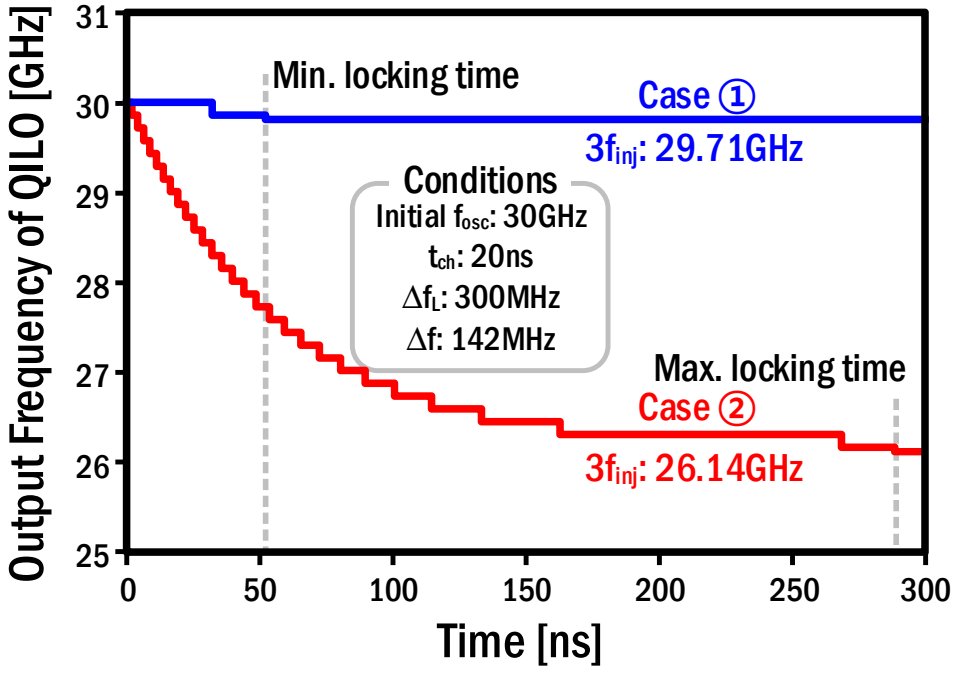
- f_{inj}= 9.43GHz ($3f_{inj}$=28.29GHz)
- Initial f_{osc}= 30.1GHz
- $f_{osc} - 3f_{inj}$ = 1.81GHz
- After locking, 1 LSB pushing for PN calibration
- Locking time: ~175ns

Locking Time Estimation

❑ Loop modeling for locking time



❑ Min. & max. locking time

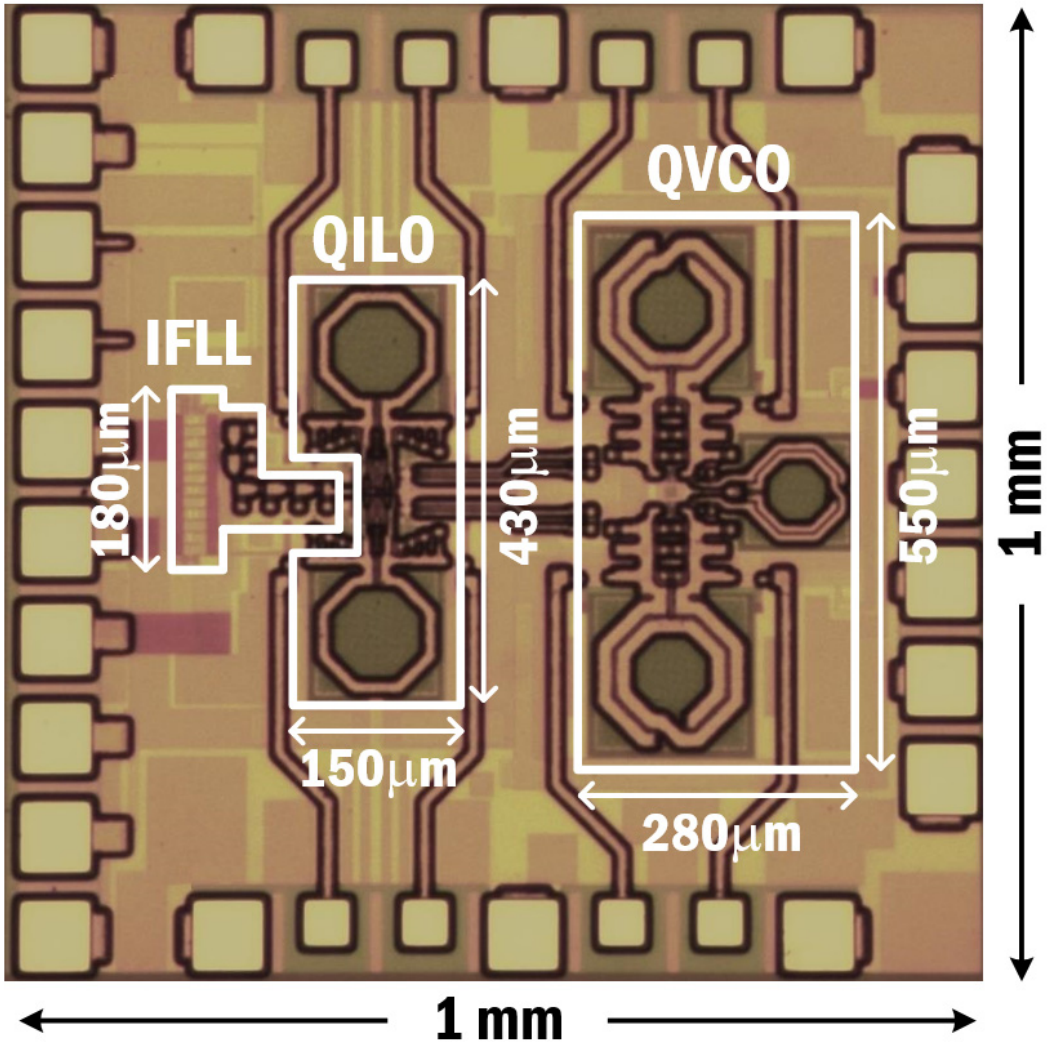


❑ Estimated locking time

$$t_{locking} = t_{disch} + \sum_{k=1}^{k=N} \frac{8}{[\{f_{osc}-3f_{inj}+(1-k)\cdot\Delta f\}^2-(\Delta f_L/2)^2]^{1/2}}, \quad N = \left\lfloor \frac{f_{osc}-(3f_{inj}+\Delta f_L/2)}{\Delta f} \right\rfloor + 1$$

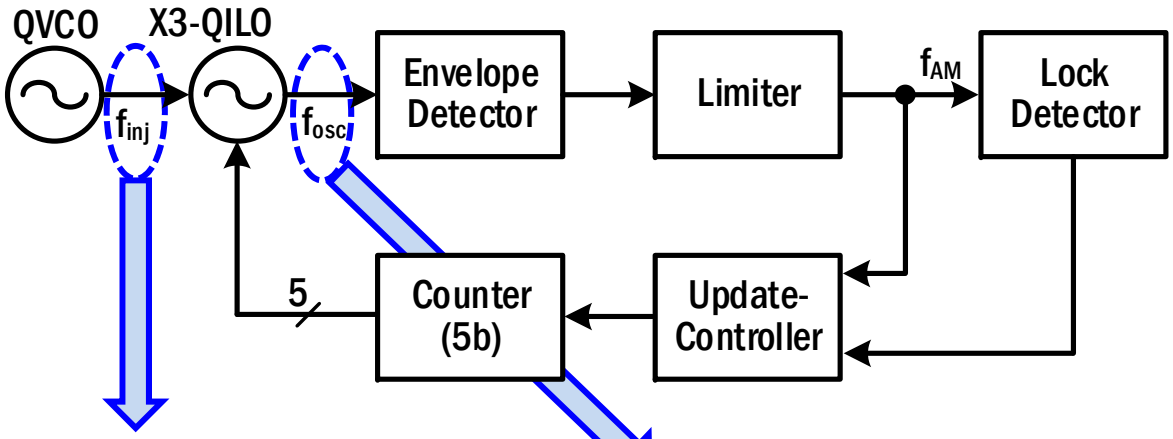
❖ t_{disch} : discharging time of Q-pump for lock signal

Chip Photograph



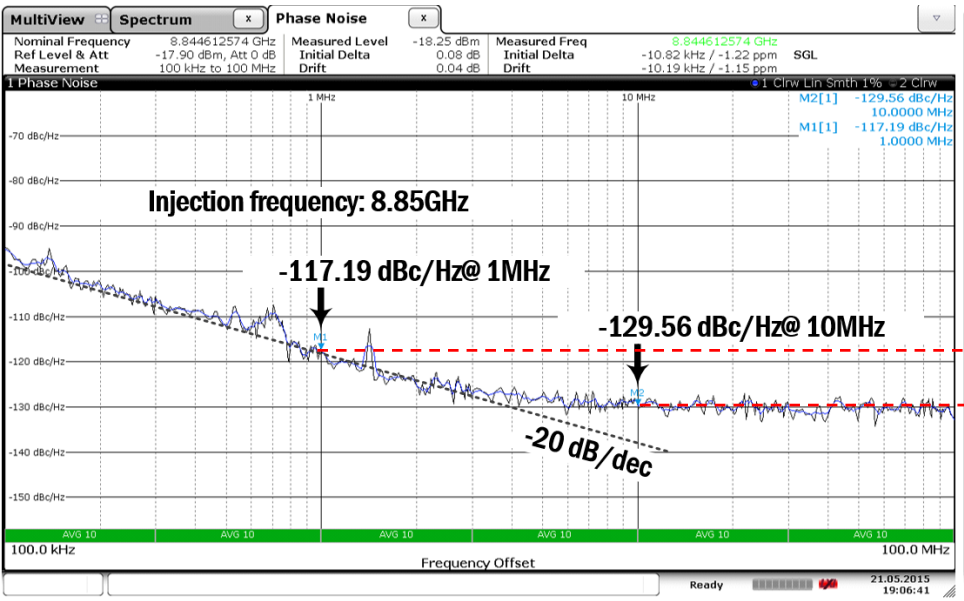
- IBM 0.13μm CMOS
- VDD: 0.9/1.3V
- Chip area: 1x1 mm^2
- IFLL area: 0.015 mm^2

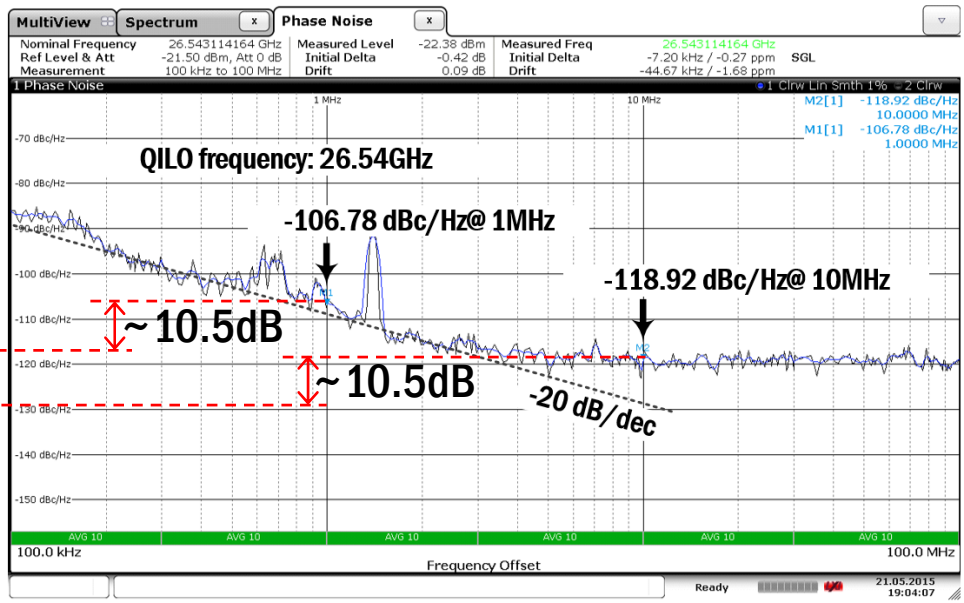
Measured Phase Noise



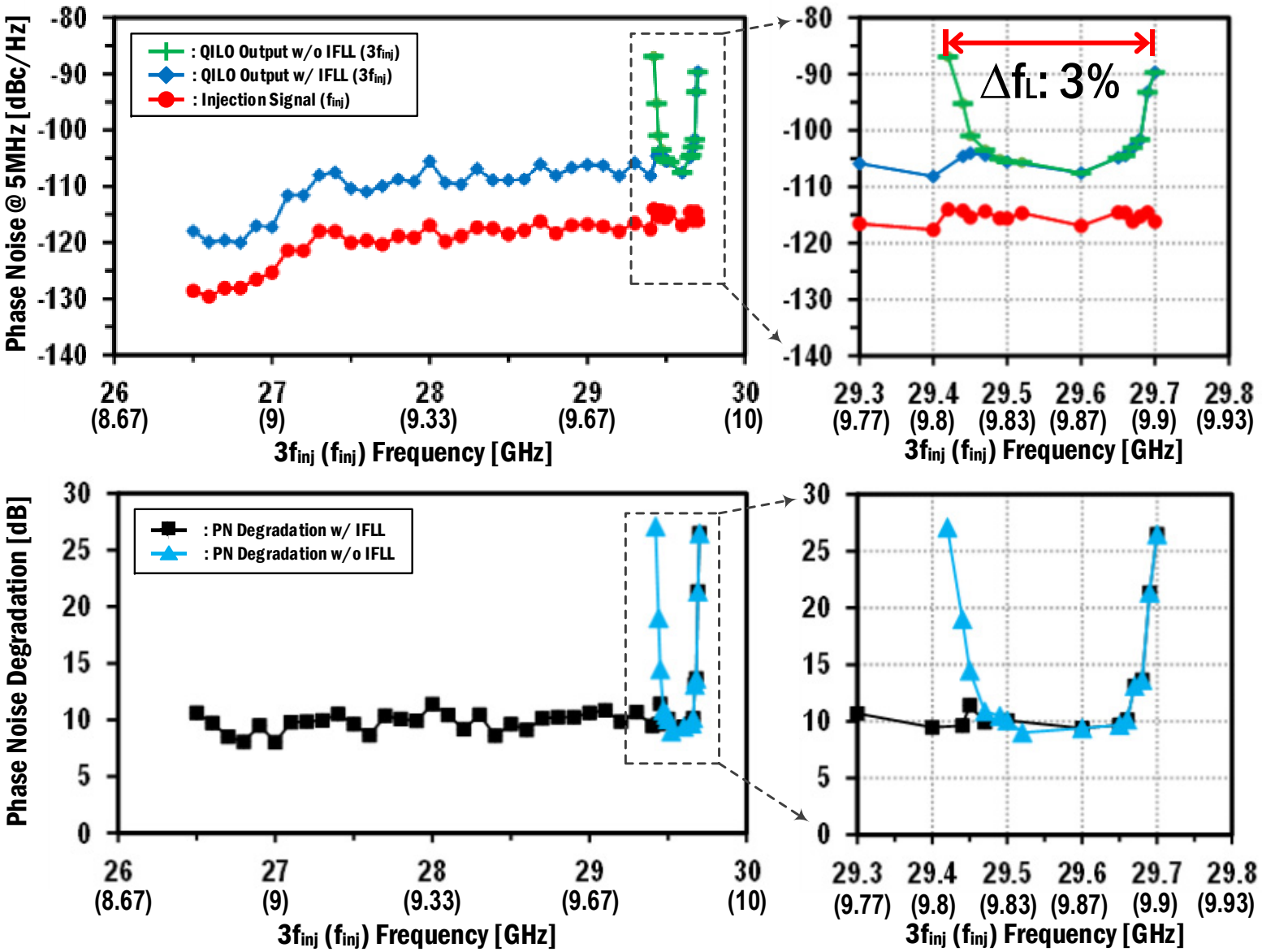
❑ Injection Frequency (8.85GHz)

❑ QILO Frequency after IFLL (26.54GHz)





Measured Phase Noise



Performance Summary and Comparison

❑ Calibration circuit comparison

	JSSC 2013 [3]	This Work
Tech	65nm CMOS	130nm CMOS
Feature	PLL+Mixer +Doulber	Envelope Detector
Locking Range (%) [w/o Calibration]	11.2 [0.5]	11.4 [1]
VDD (V)	1.2	1.3
Power (mW)	65	2.4 (27x)
Area (mm^2)	~ 0.95*	0.015 (63x)
Locking Time	< 42.7us	<**300ns (142x)
Operation	Externally Controlled	Autonomous

*Estimation based on chip photograph.
**Estimation based on simulations.

❑ Comparison with prior state-of-the-art works

	ISSCC 2013[5]	JSSC 2011[4]	JSSC 2013 [3]	This Work
Tech	130nm SiGe	65nm CMOS	65nm CMOS	130nm CMOS
Phase	Diff.	Quad.	Quad.	Quad.
Frequency (GHz)	27.9 -37.8	67.2- 67.7	58.1-65	26.5 -29.7
VDD (V)	1.5	1.2	1.2	1.3
Power (mW)	10 (VCO only)	68	137	*38.6 (**49.7)
Phase Noise (dBc/Hz@1MHz offset)	-103.6 @32.9GHz	-95 @60GHz	-96 @61.5GHz	-106.8 @26.5GHz
Chip Area (mm^2)	1.93	0.8 (QILO only)	3.8	1
Feature	BiCMOS Cross-coupled Pair VCO	PLL+QILO w/ Dual Injection	PLL+QILO + Calibration Circuit	QVCO+QILO + Calibration Circuit

*Without VCO output buffers.
**With including VCO output buffers for measurement with 50-W instruments.

Conclusion

- **LO Signal Generator : QVCO + QILO + IFLL**
  - QVCO: 8.8-to-10GHz
  - QILO w/ IFLL: 26.5-to-29.7GHz (Δf_L : 11.4%)
- **Proposed IFLL**
  - Autonomous calibration in digital domain
  - Fast locking time, less than 300ns
  - Low power consumption (2.4mW) and small area (0.015mm^2)
  - No PN degradation at the edge of Δf_L
  - Suitable for low-power mm-Wave LO generation

Acknowledgements

- This work was supported in part by the Ministry of Trade, Industry and Energy (MOTIE) grant funded by the Korean government (No. 10050527).

A 2GHz 244fs-Resolution 1.2ps-Peak-INL Edge-Interpolator-Based Digital-to-Time Converter in 28nm CMOS

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R. Banin[2], A. Ravi[3], B.-U. Klepser[1],
Z. Boos[1], D. Schmitt-Landsiedel[4]

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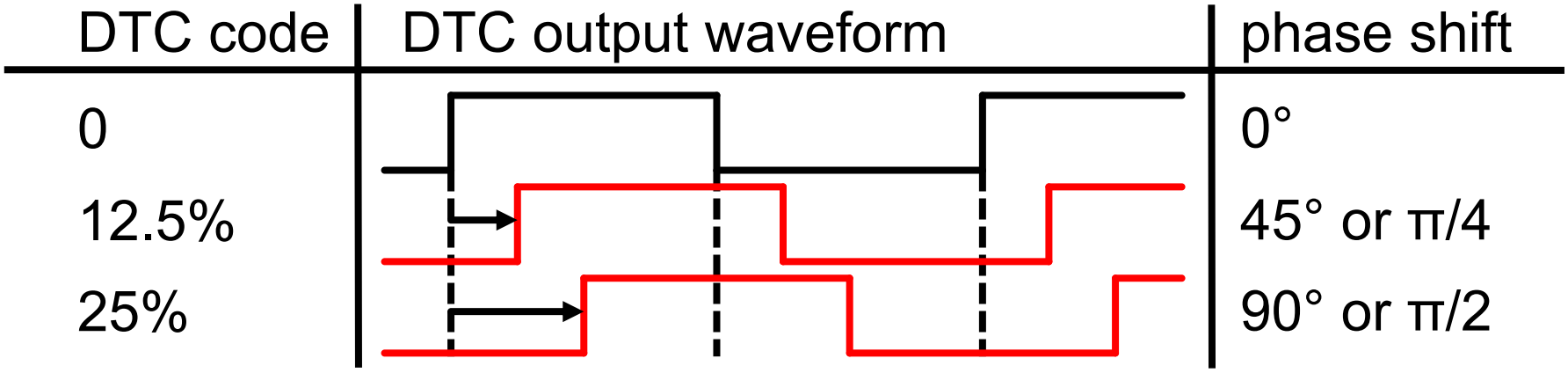
[4]Technische Universität München (TUM), Munich, Germany

Outline

1. Introduction to Digital-to-Time Converters
2. DTC Architecture and Design
   - Linearized Phase Interpolator
3. Measurement Results
4. Summary

1. Introduction to Digital-to-Time Converters (1/3)

- Digital-to-time converters (DTC) generate a clock with a time delay (or phase shift) based on a digital input code
- DTCs are usually driven by a reference clock
- Example for DTC operation:



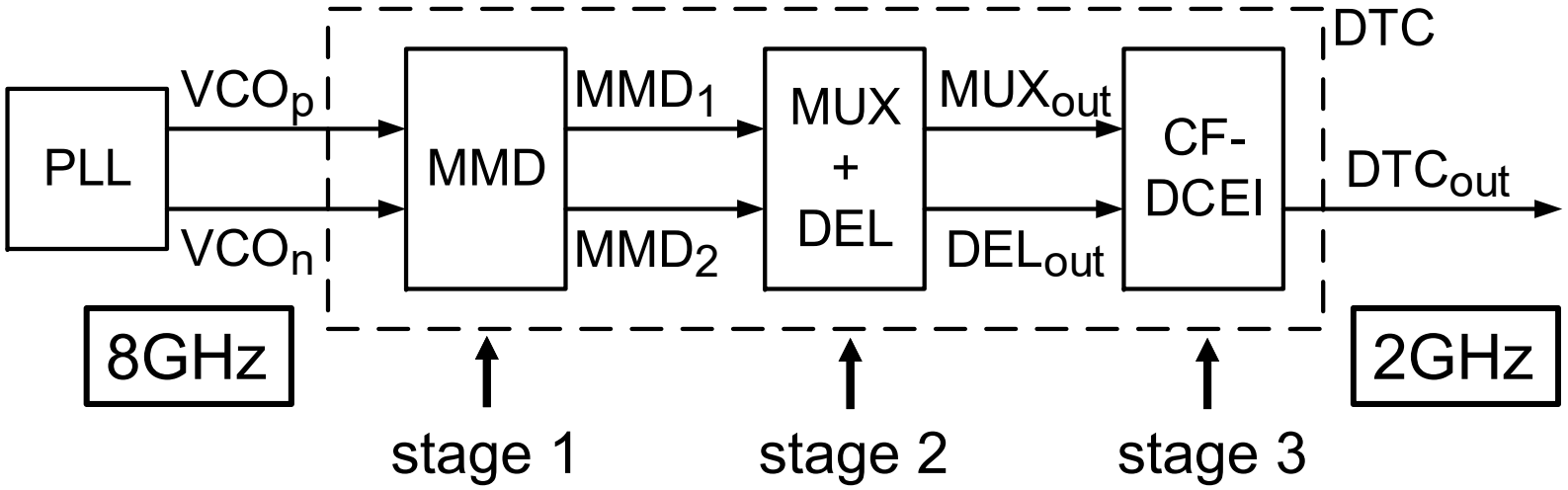
1. Introduction to Digital-to-Time Converters (2/3)

- Examples of use cases:
  1. Tune the sampling clock in clock-and-data-recovery (CDR) circuits [1,2]
  2. In the feedback or reference path of a phase-locked loop (PLL) to relax phase detector requirements [3,4]
  3. As direct phase modulator in outphasing transmitters [5]
- DTCs are often built in a segmented fashion, where each stage provides successively finer time resolution

1. Introduction to Digital-to-Time Converters (3/3)

- The presented DTC design employs:
  - Divider based coarse tuning
  - Linearized phase interpolator based fine tuning
- The DTC‘s reference clock of 8GHz is generated by a chip internal PLL
- The DTC generates a 2GHz output signal with adjustable phase
- 11b digital resolution yield in 244fs time resolution

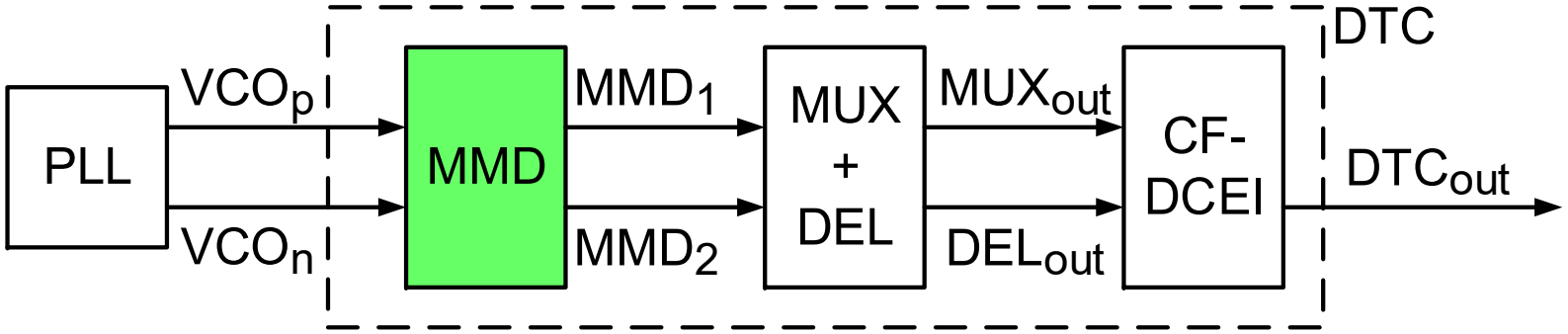
2.1 DTC Architecture and Design

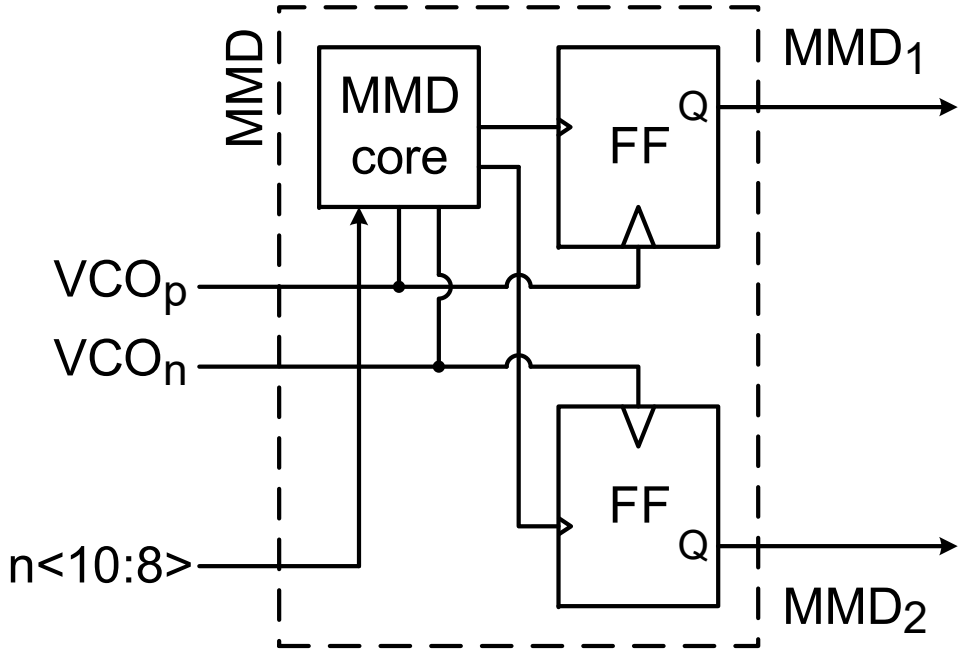


- DTC implemented as 11b, 3 stage architecture
  - Each stage provides successively finer resolution

Stage	MMD	MUX+DEL	CF-DCEI
Resolution	3b	1b	7b
	62.5ps (45°)	31.25ps (22.5°)	244fs (0.18°)

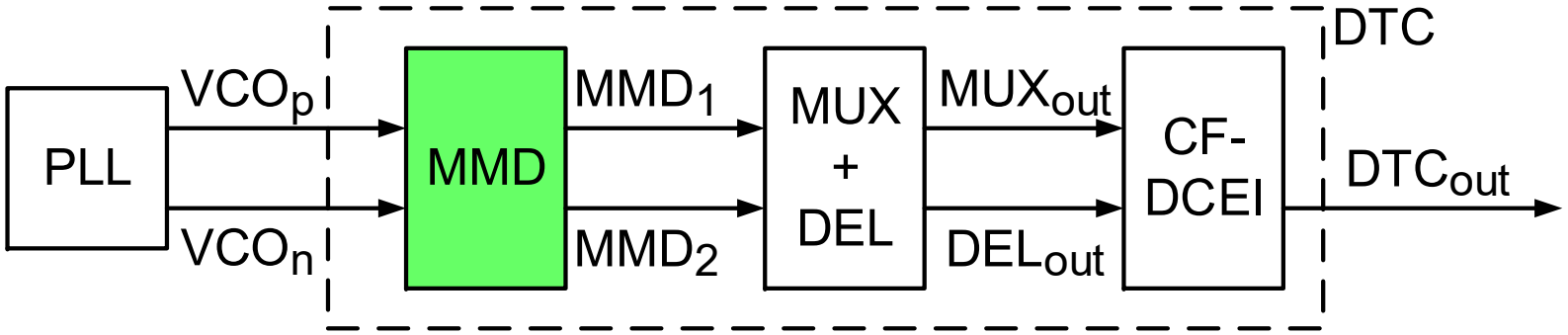
2.2 Multi-Modulus Divider (1/4)





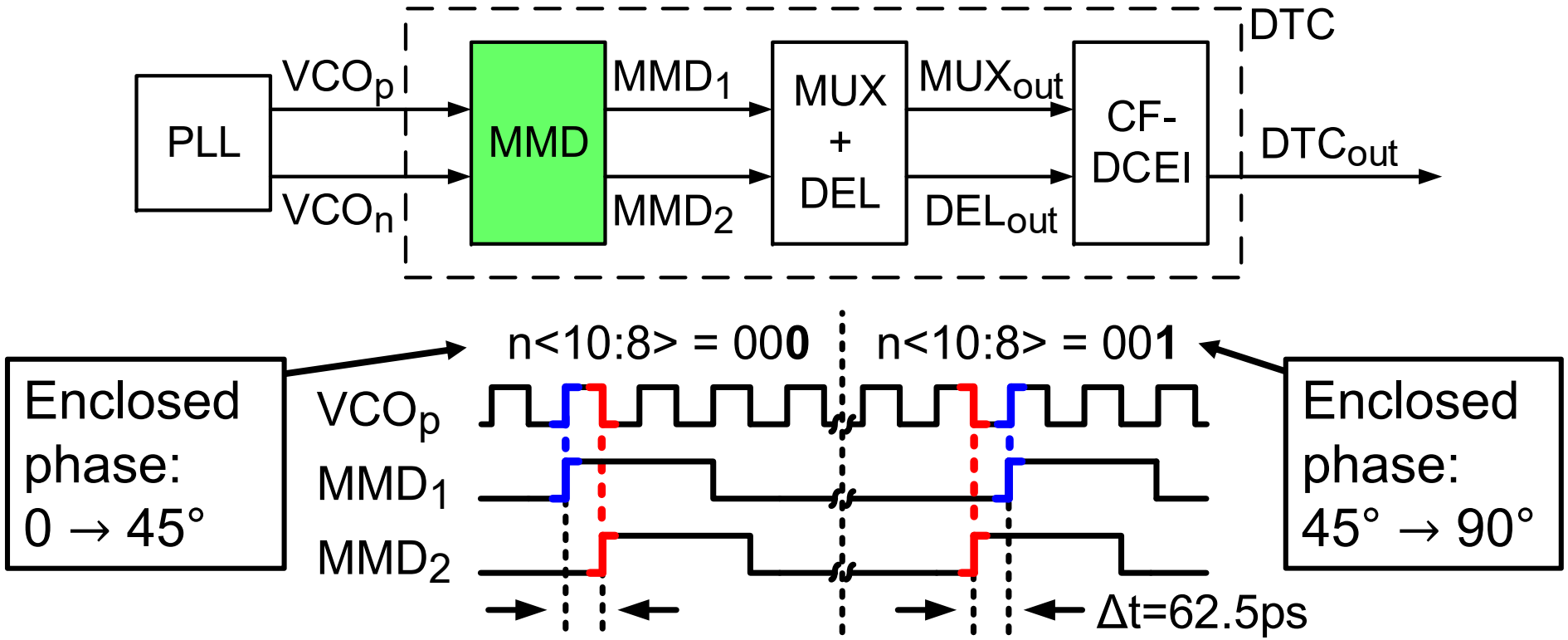
- 3b multi-modulus divider (MMD)
  - Can divide by 3,4, or 5
- Nominal division ratio is 4
  - 8GHz VCO leads to 2GHz DTC output
- Outputs enclose, depending on code n, different 45° = π/4 wide parts of the 2π period

2.2 Multi-Modulus Divider (2/4)



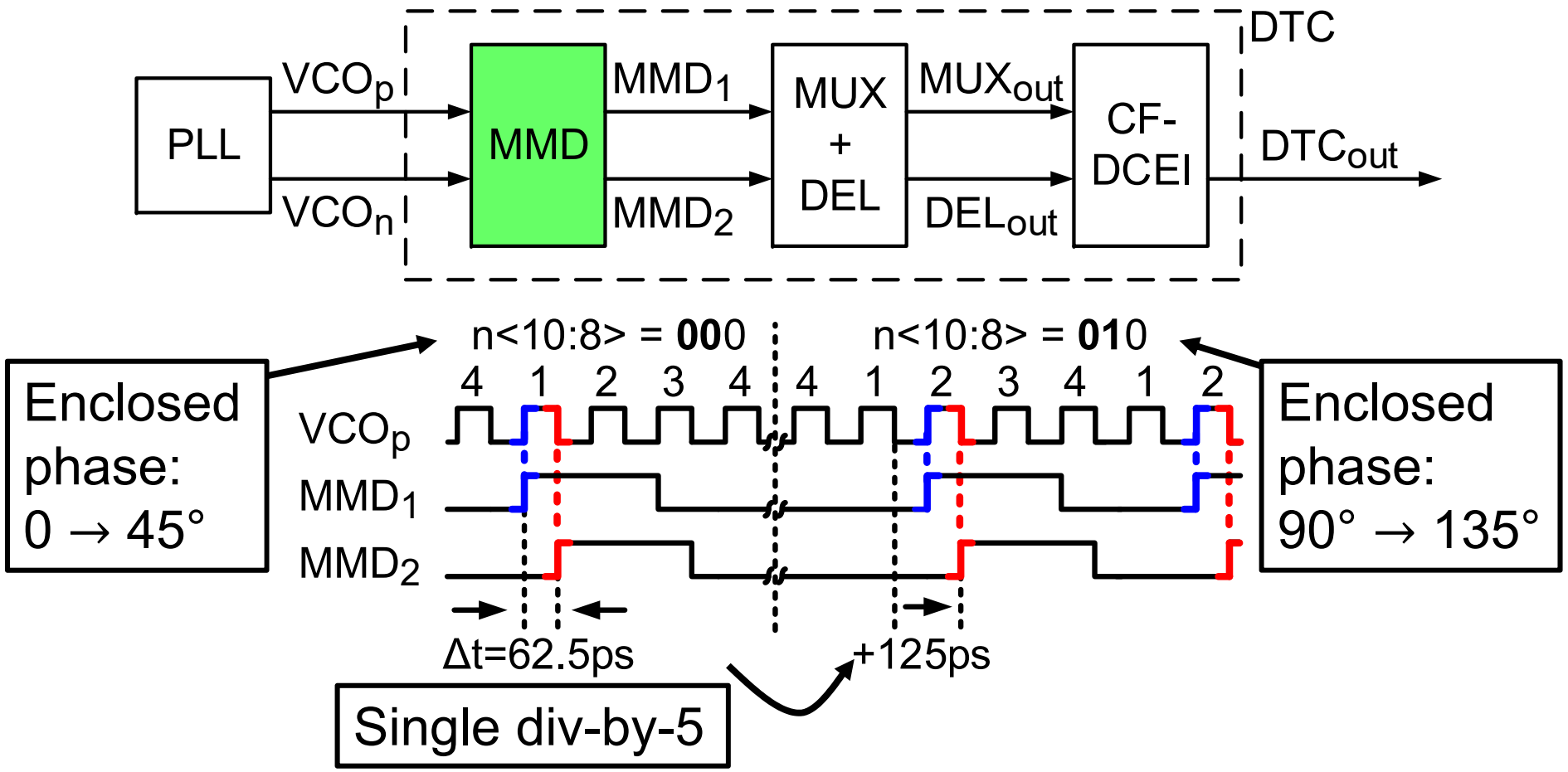
2 GHz Reference		
n<10:8> = 0	MMD_1 MMD_2	
n<10:8> = 1	MMD_1 MMD_2	
⋮	⋮	⋮
n<10:8> = 7	MMD_1 MMD_2	

2.2 Multi-Modulus Divider (3/4)



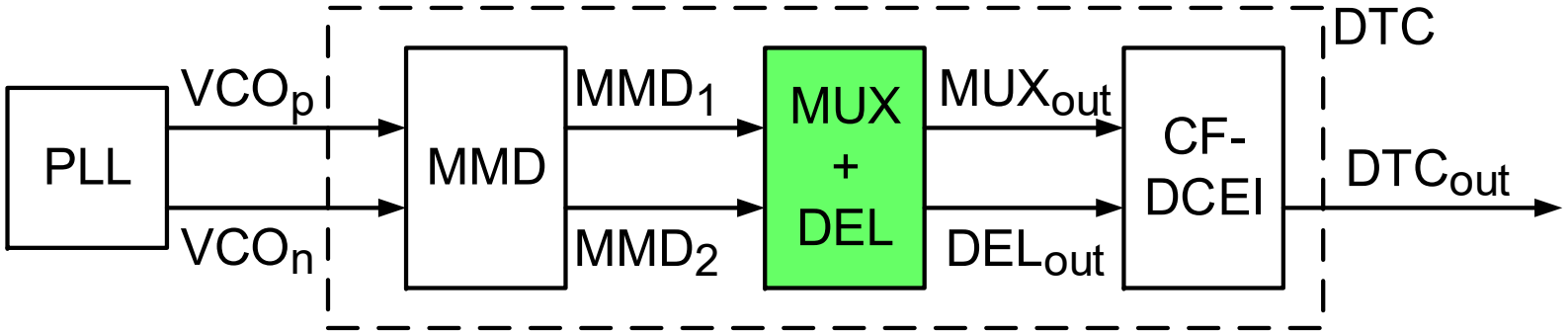
- MMD_1 is aligned with VCO_p, MMD_2 with VCO_n
- n_8 controls if MMD_1 is aligned with either VCO_p directly leading or lagging VCO_n of MMD_2

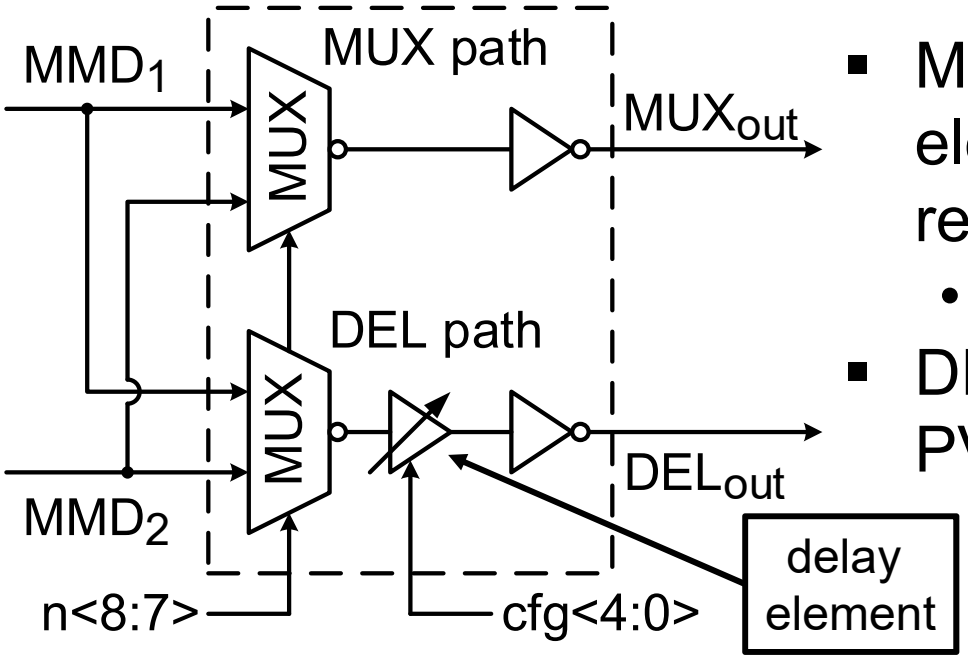
2.2 Multi-Modulus Divider (4/4)



- With a single division by 3 or 5, MMD_2 can be re-aligned with a neighbouring relative VCO cycle

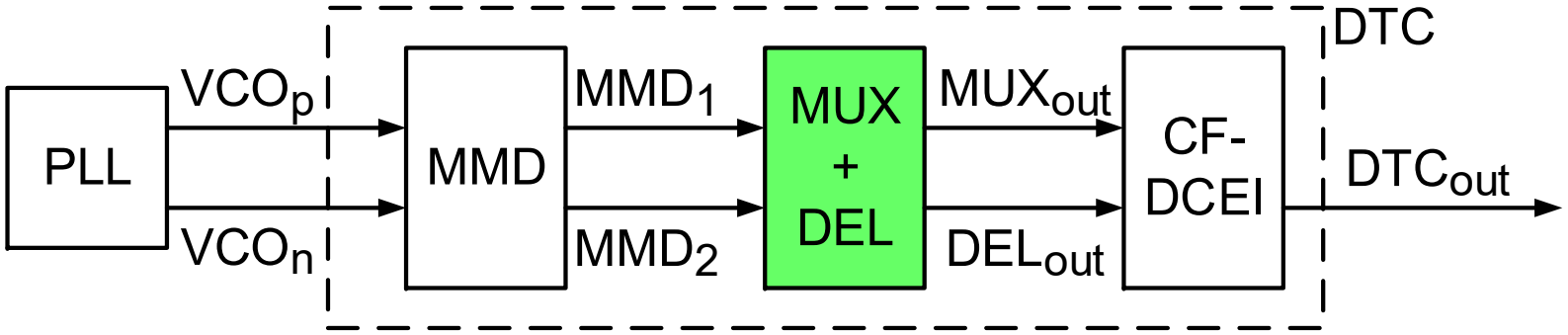
2.3 Multiplexer and Delay (1/2)

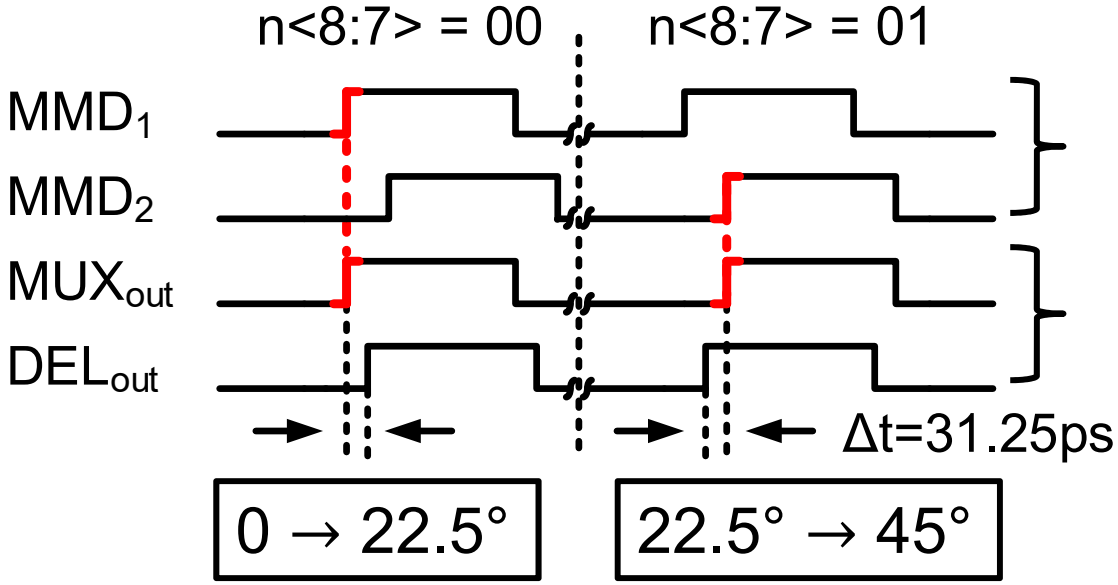




- Multiplexer (MUX) and a delay element (DEL) are used to reduce the spacing
  - 62.5ps reduced to 31.25ps
- DEL can be configured for PVT to have ~31.25ps delay

2.3 Multiplexer and Delay (2/2)



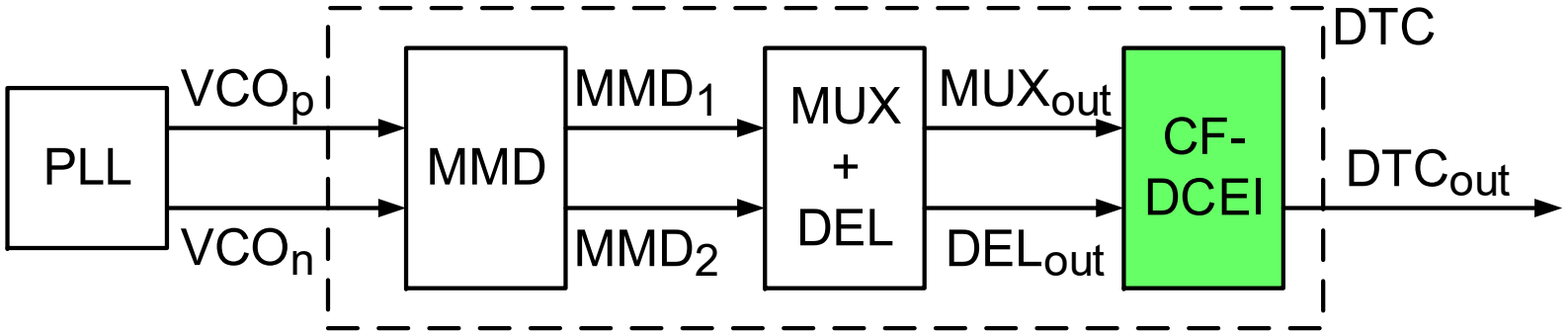


$MMD_{1/2}$ enclose
62.5ps = 45°

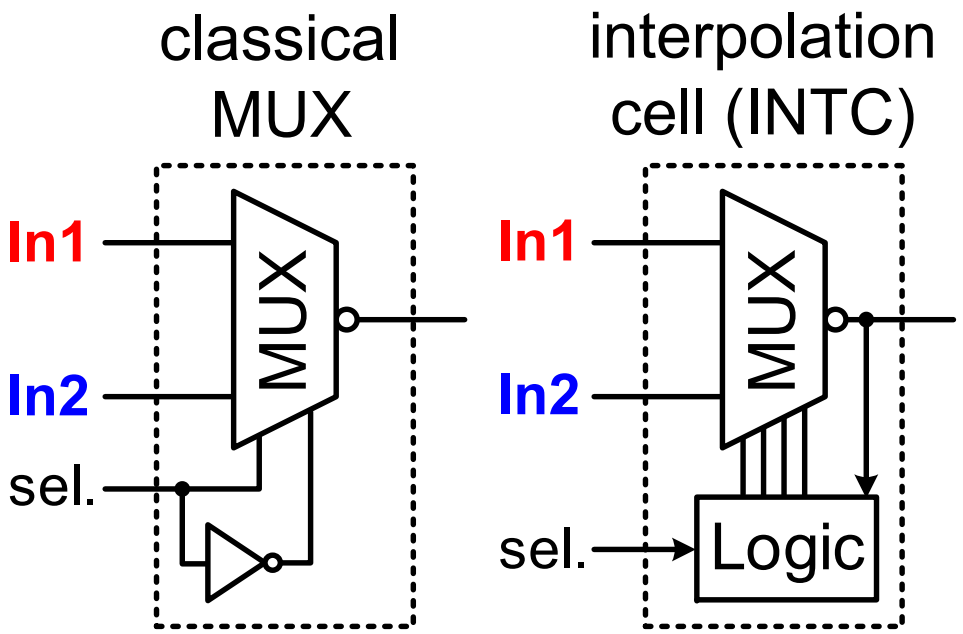
MUX/DEL_{out} enclose
31.25ps = 22.5°

- MUX path can select either the early or late MMD output
- DEL path delays always the earlier MMD output by 31.25ps

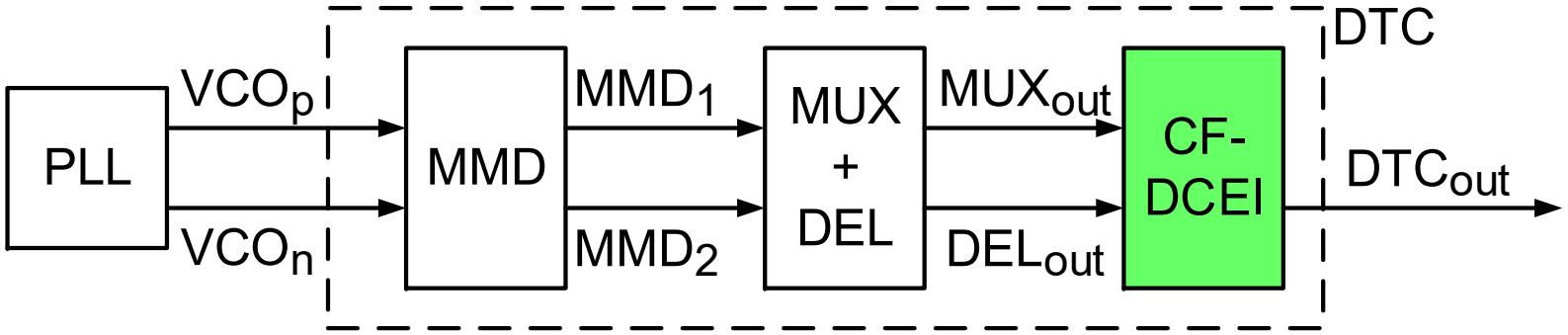
2.4 Phase Interpolator (1/3)



- 7b edge interpolation, i.e. interpolation on dig. signals
- Contention-free digitally controlled edge interpolator (CF-DCEI)
- 2^7=128 MUX like cells are used for interpolation, each either weighting the 1st or 2nd input of the CF-DCEI



2.4 Phase Interpolator (2/3)



- 7b edge interpolation, i.e. interpolation on dig. signals
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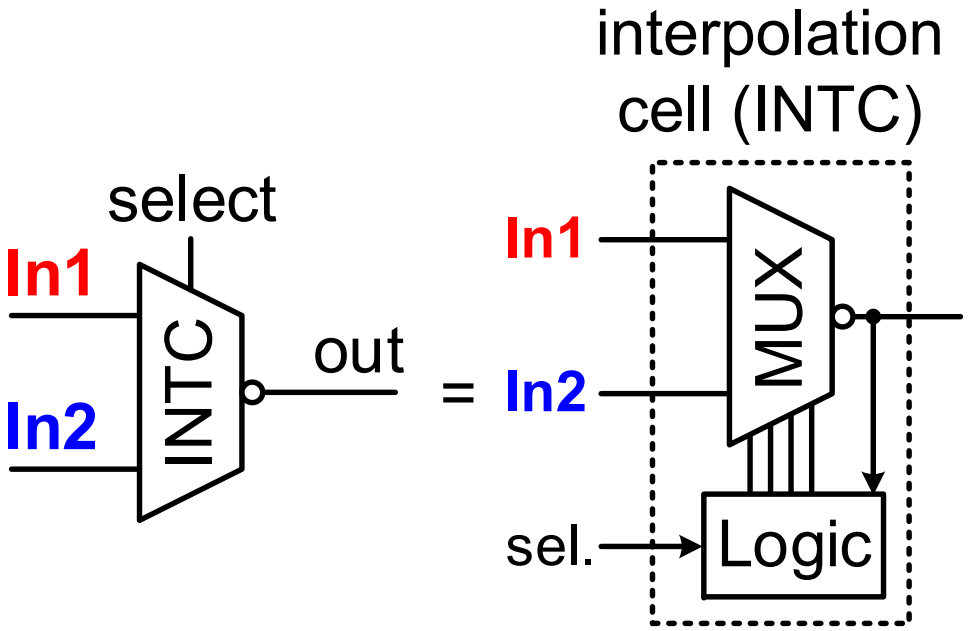
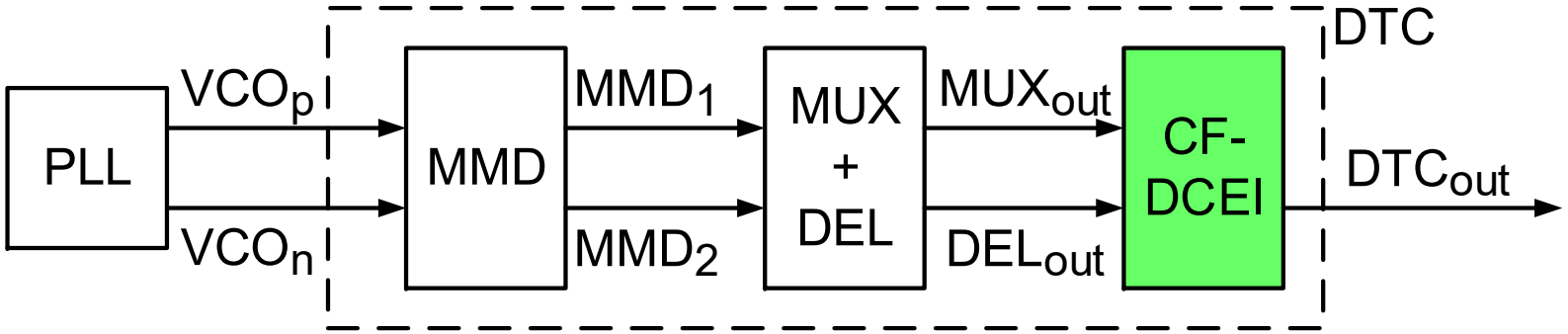
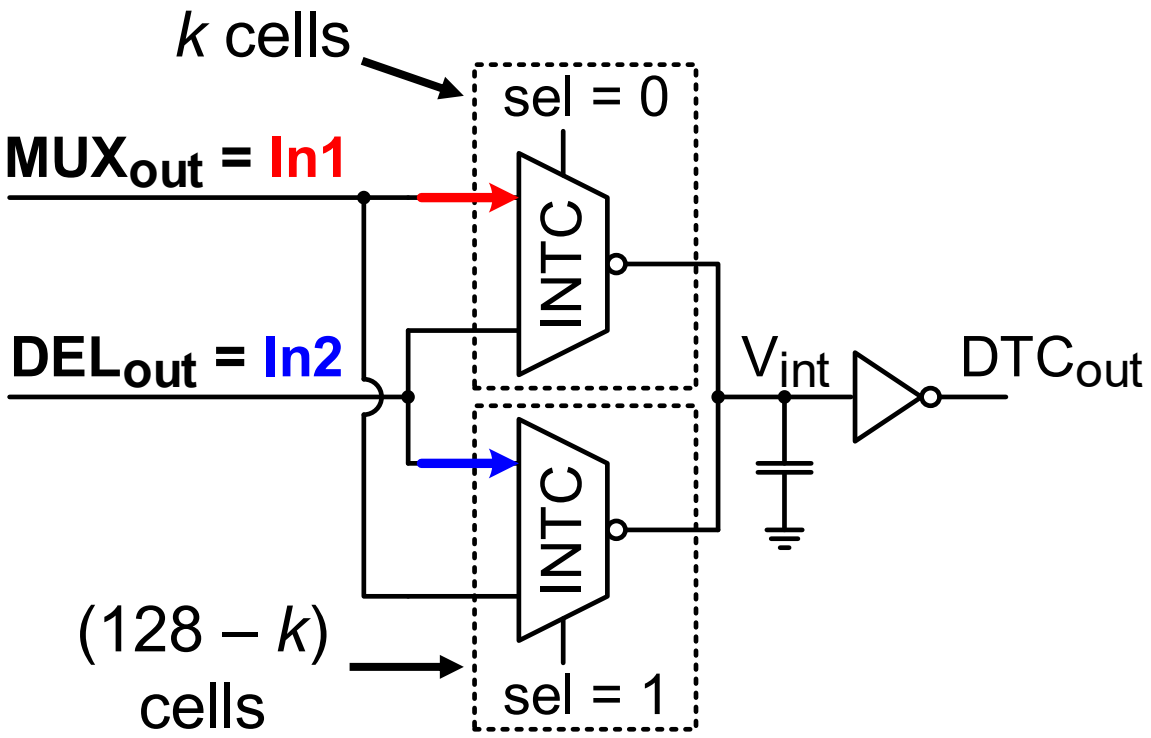


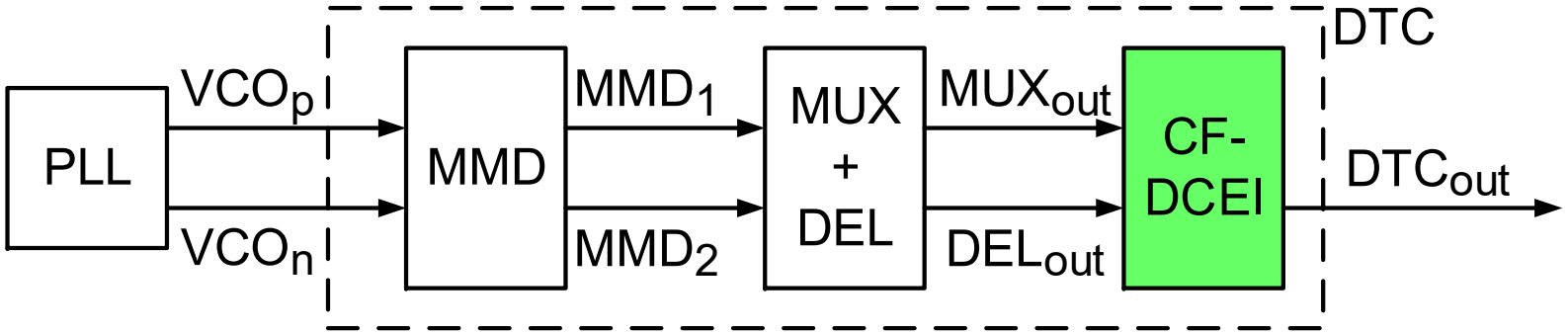
2.4 Phase Interpolator (3/3)

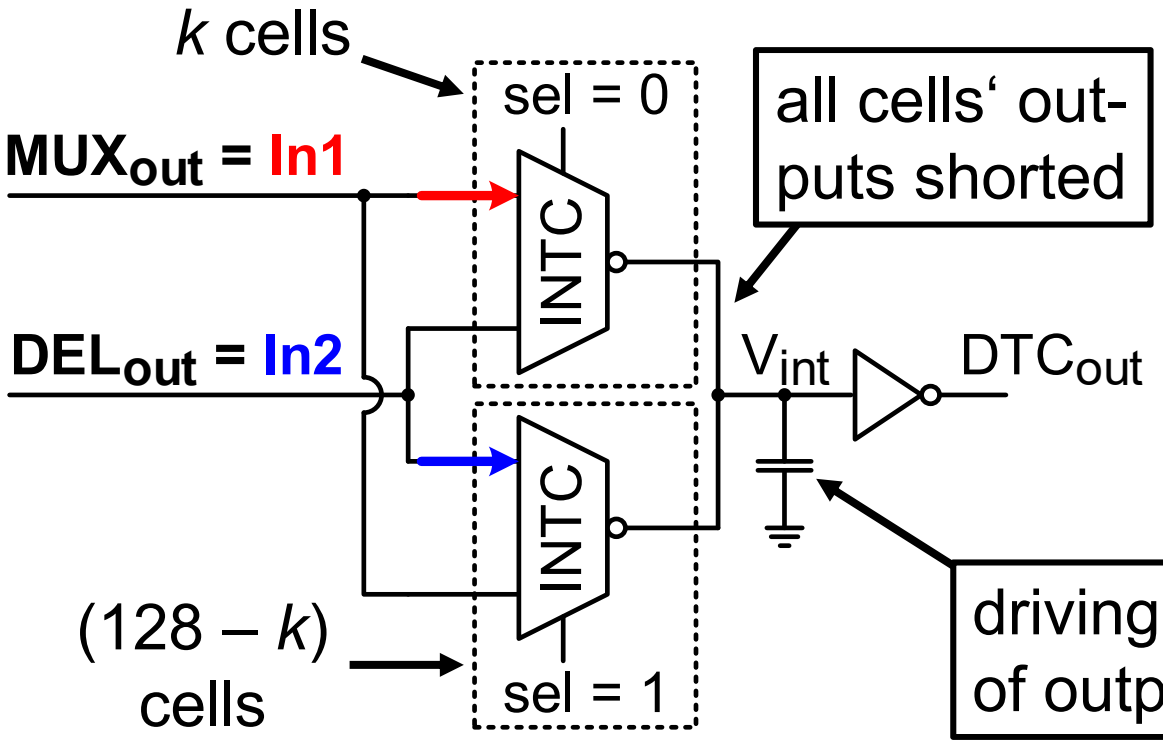




- 128 cells in total
- Organized in 8x16 cell array
- k cells weight **In1** during interpolation
- $(128 - k)$ cells weight **In2**
- $0 \leq k \leq 128$

2.4 Phase Interpolator (3/3)

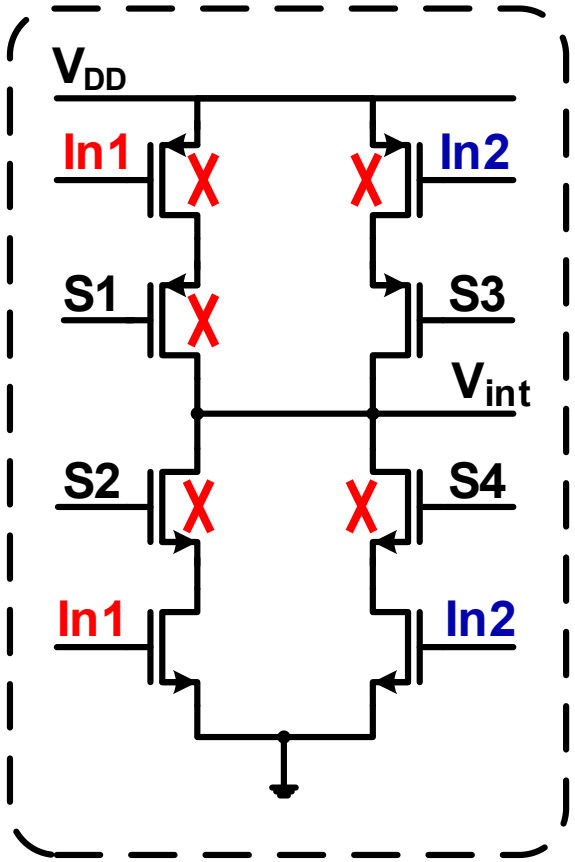




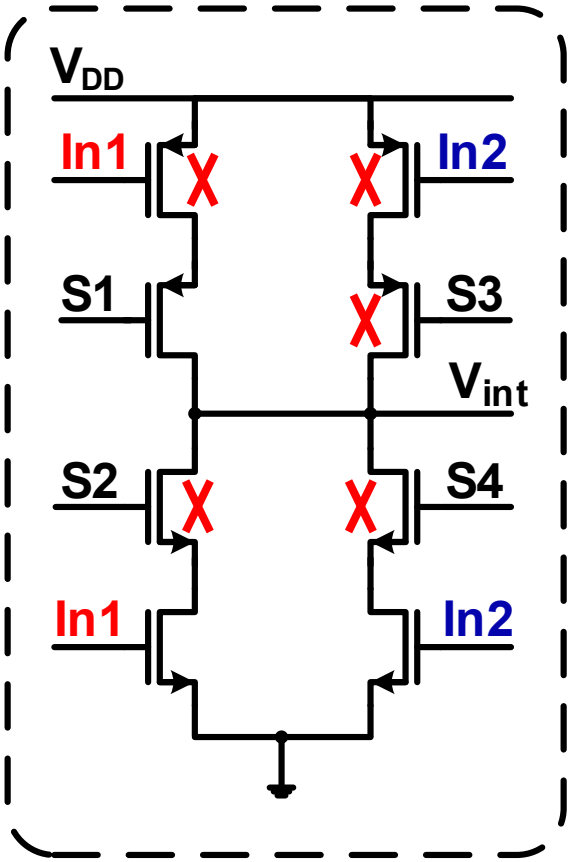
- 128 cells in total
- Organized in 8x16 cell array
- *k* cells weight **In1** during interpolation
- (128 – *k*) cells weight **In2**
- $0 \leq k \leq 128$

2.5 Linearized Interpolation (1/4)

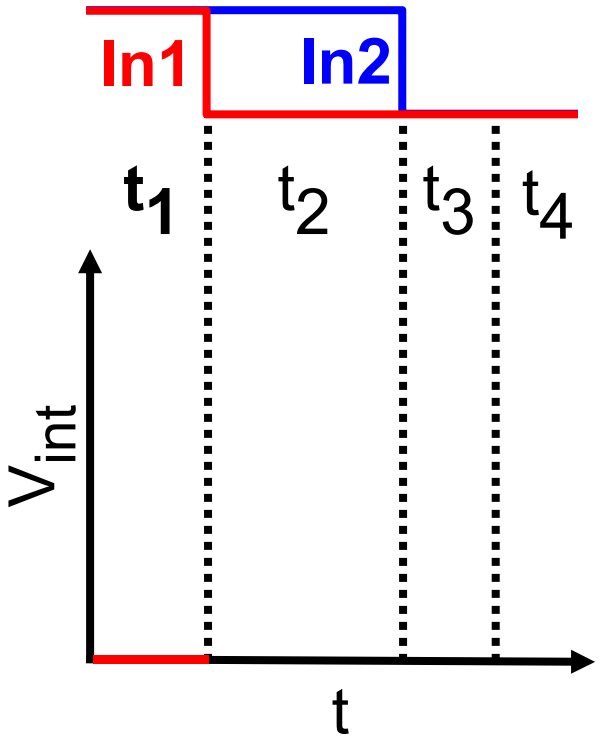
Interpolation cell
(128 - *k*)



Interpolation cell
k

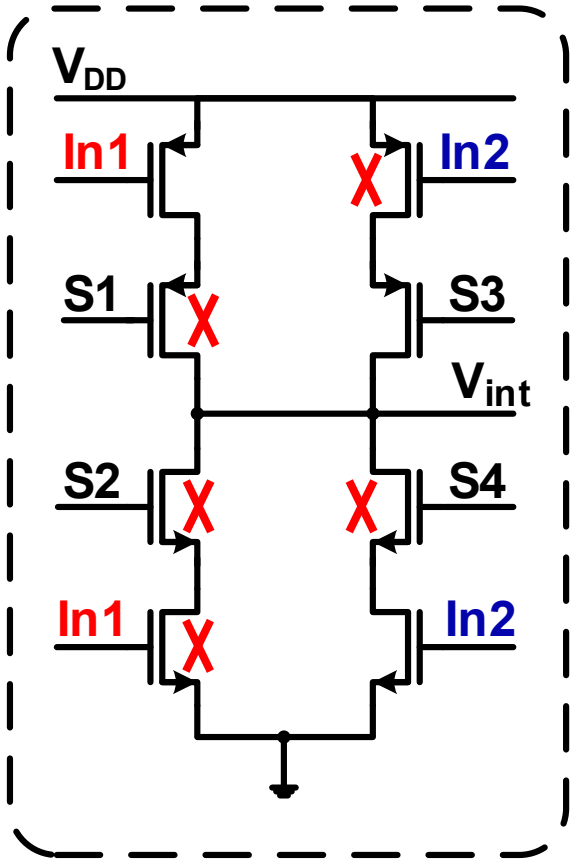


Interp. process

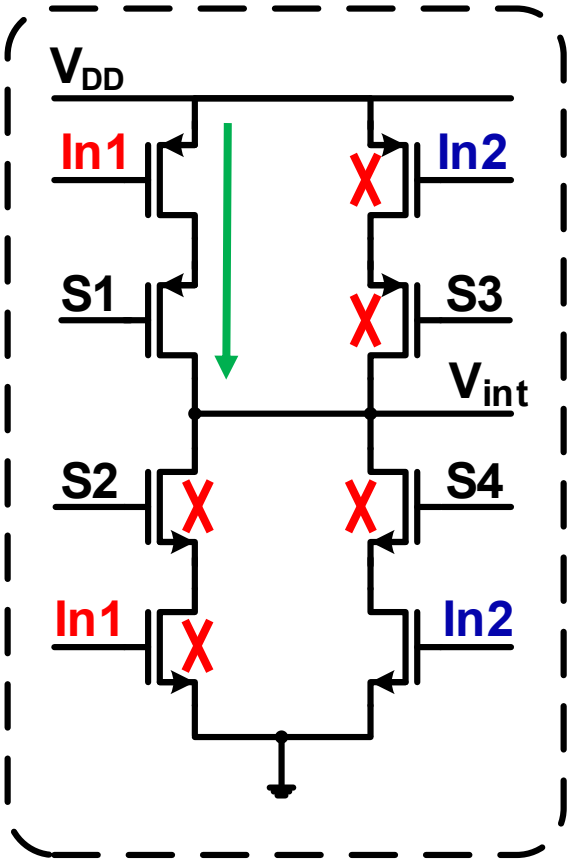


2.5 Linearized Interpolation (2/4)

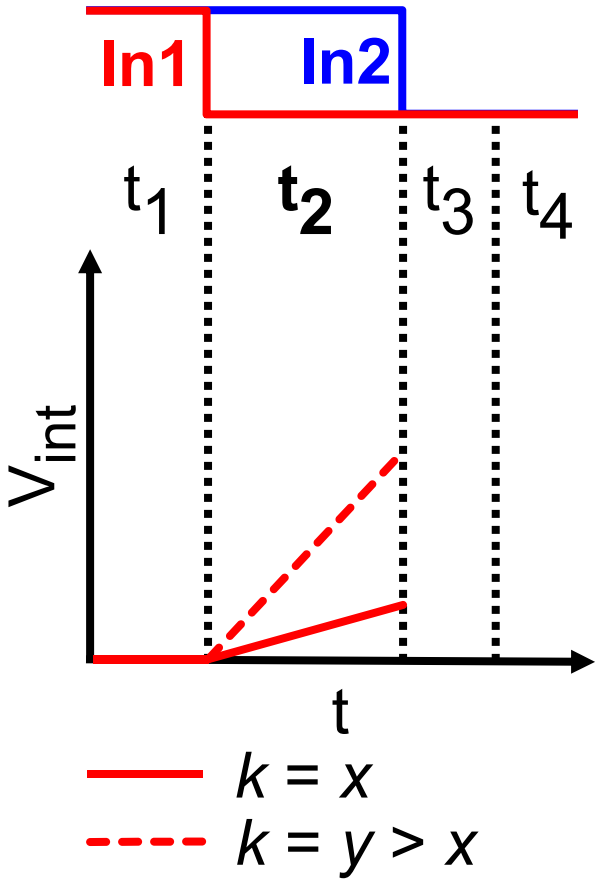
Interpolation cell
(128 - *k*)



Interpolation cell
k

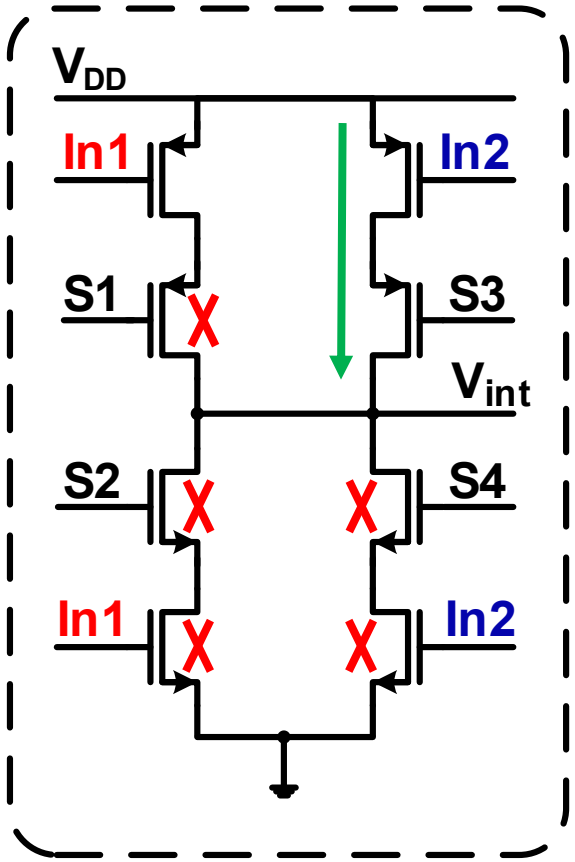


Interp. process

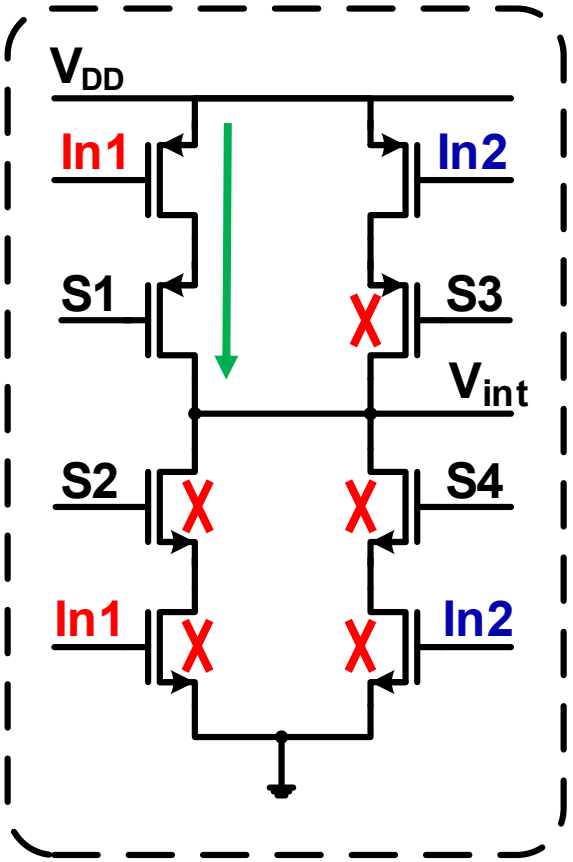


2.5 Linearized Interpolation (3/4)

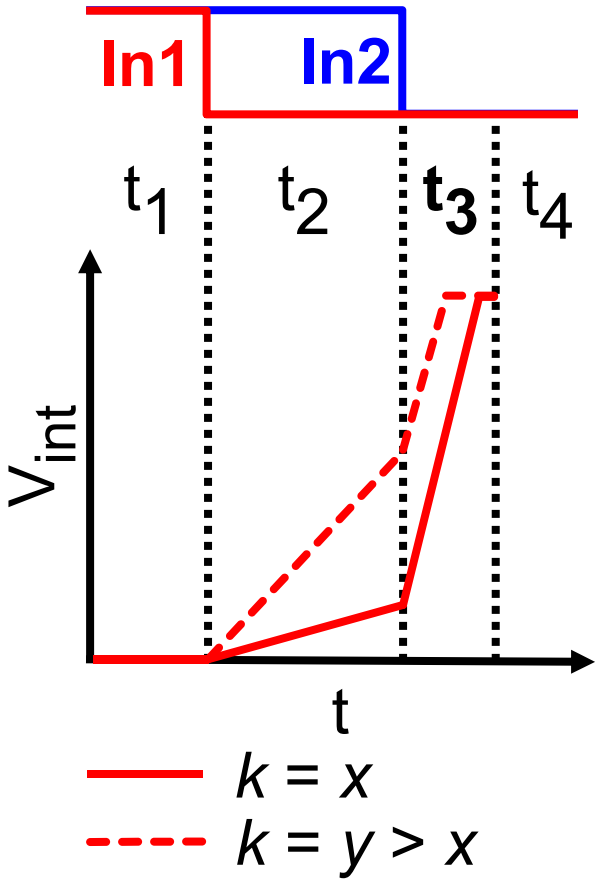
Interpolation cell
(128 - *k*)



Interpolation cell
k



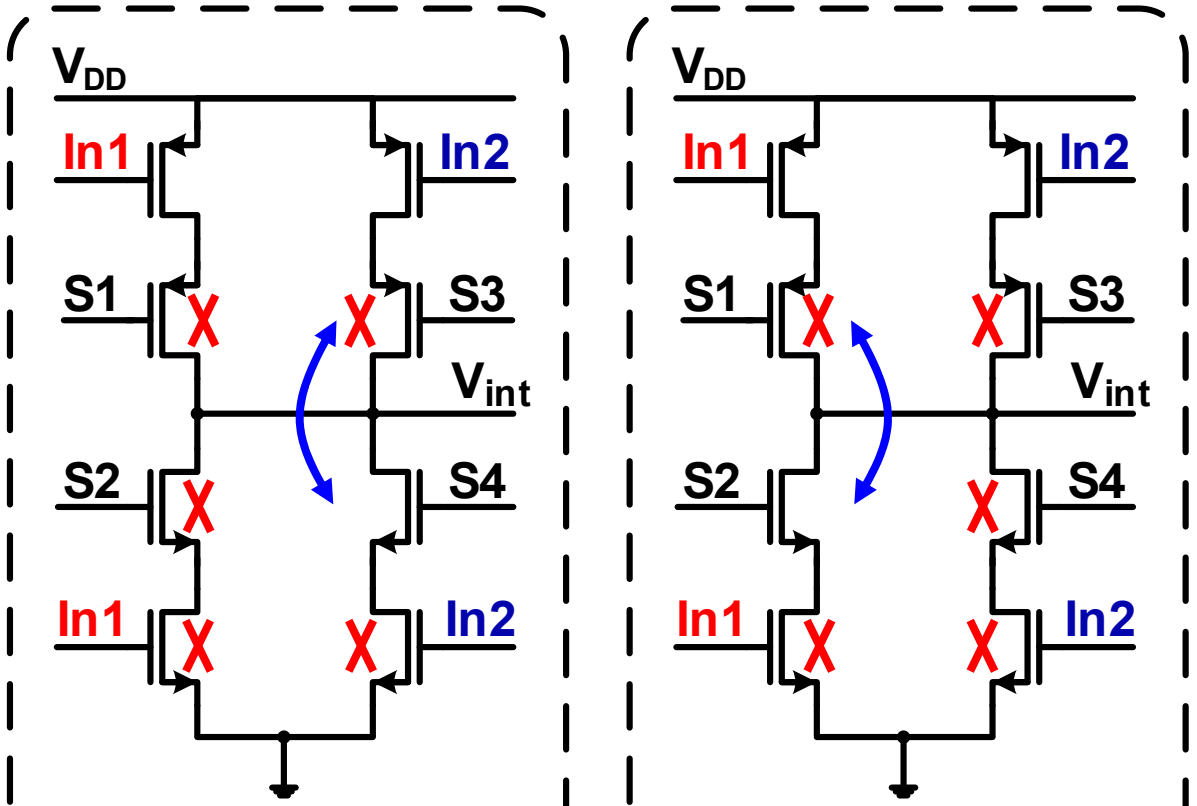
Interp. process



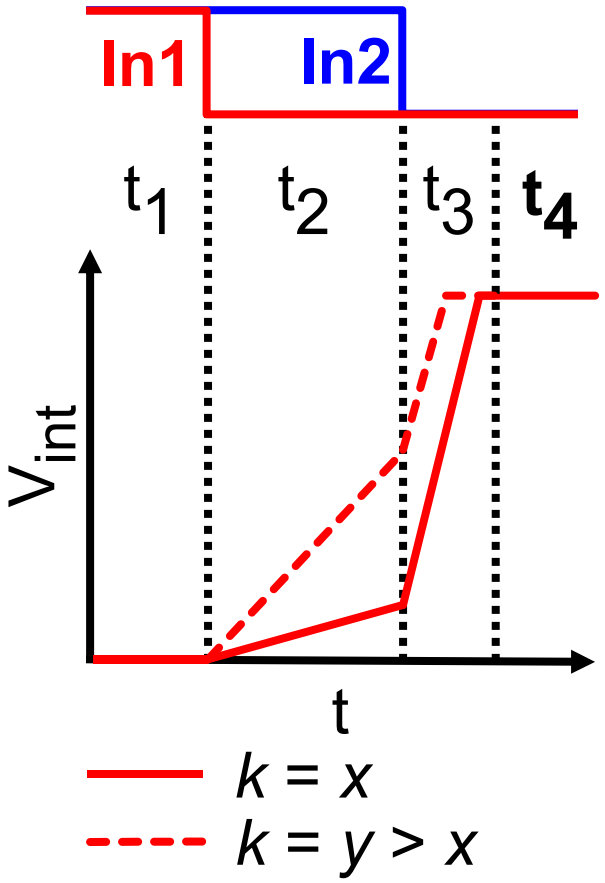
2.5 Linearized Interpolation (4/4)

Interpolation cell (128 - *k*)

Interpolation cell *k*

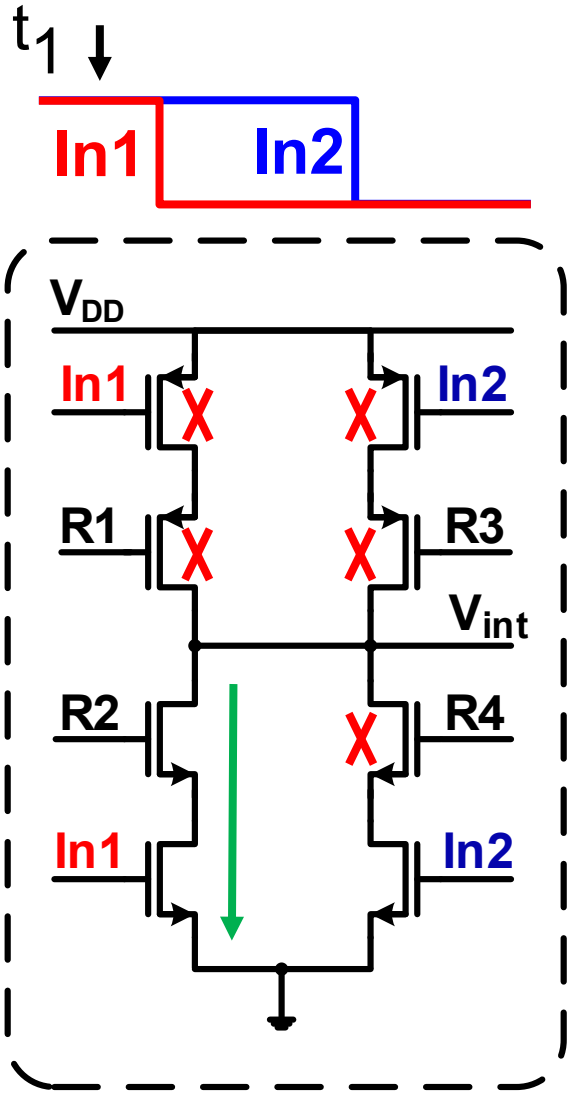


Interp. process



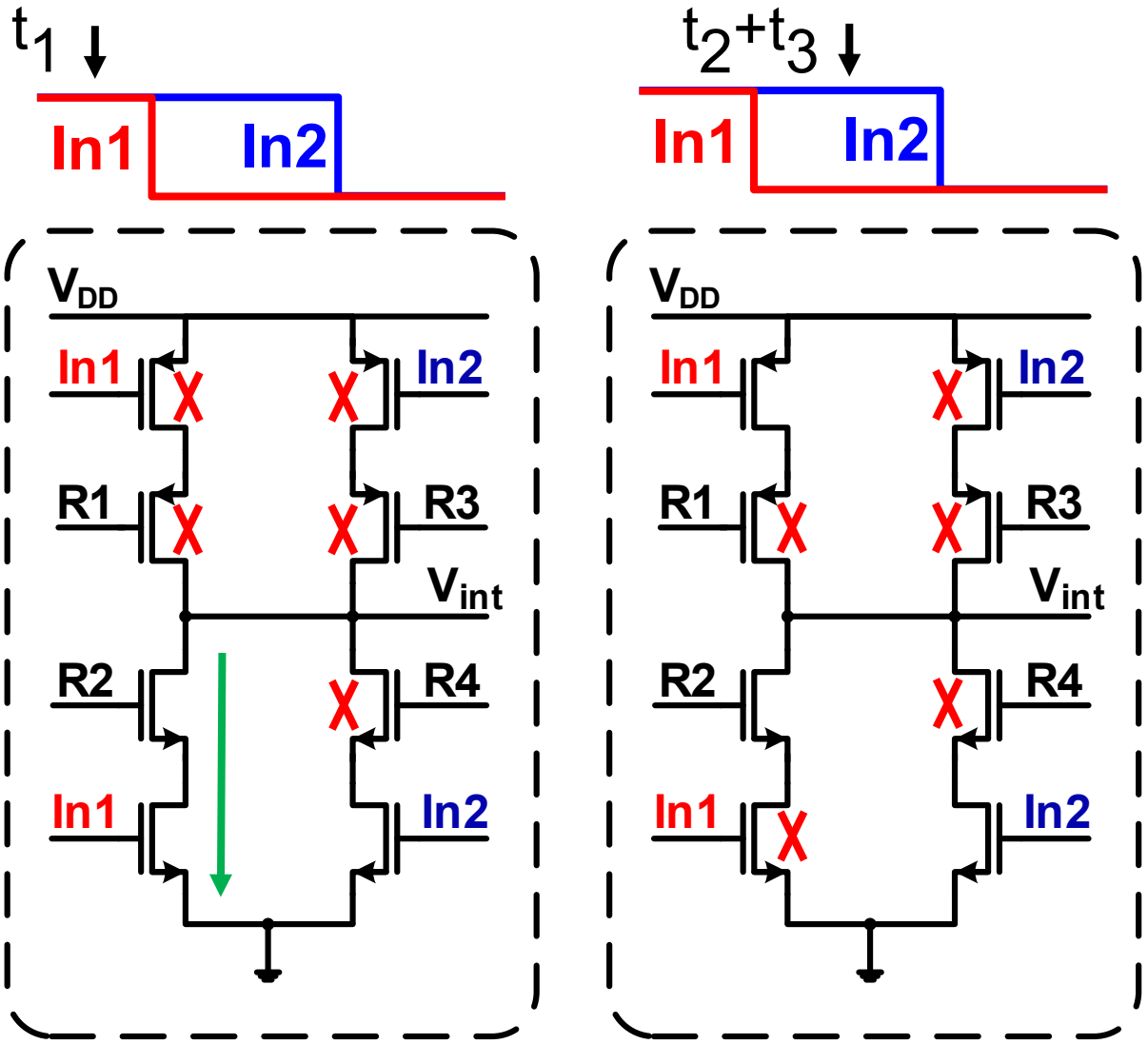
Cell internal logic switches S1,3 to S2,4 with feedback from V_{int}

2.6 Retention Cells (1/3)



- Retention cell implementation is similar to interpolation cell, only the select logic is different
  - R1-4 instead of S1-4
- Interpolation cell: First switching input starts interpolation
- Retention cell: First switching input stops retention

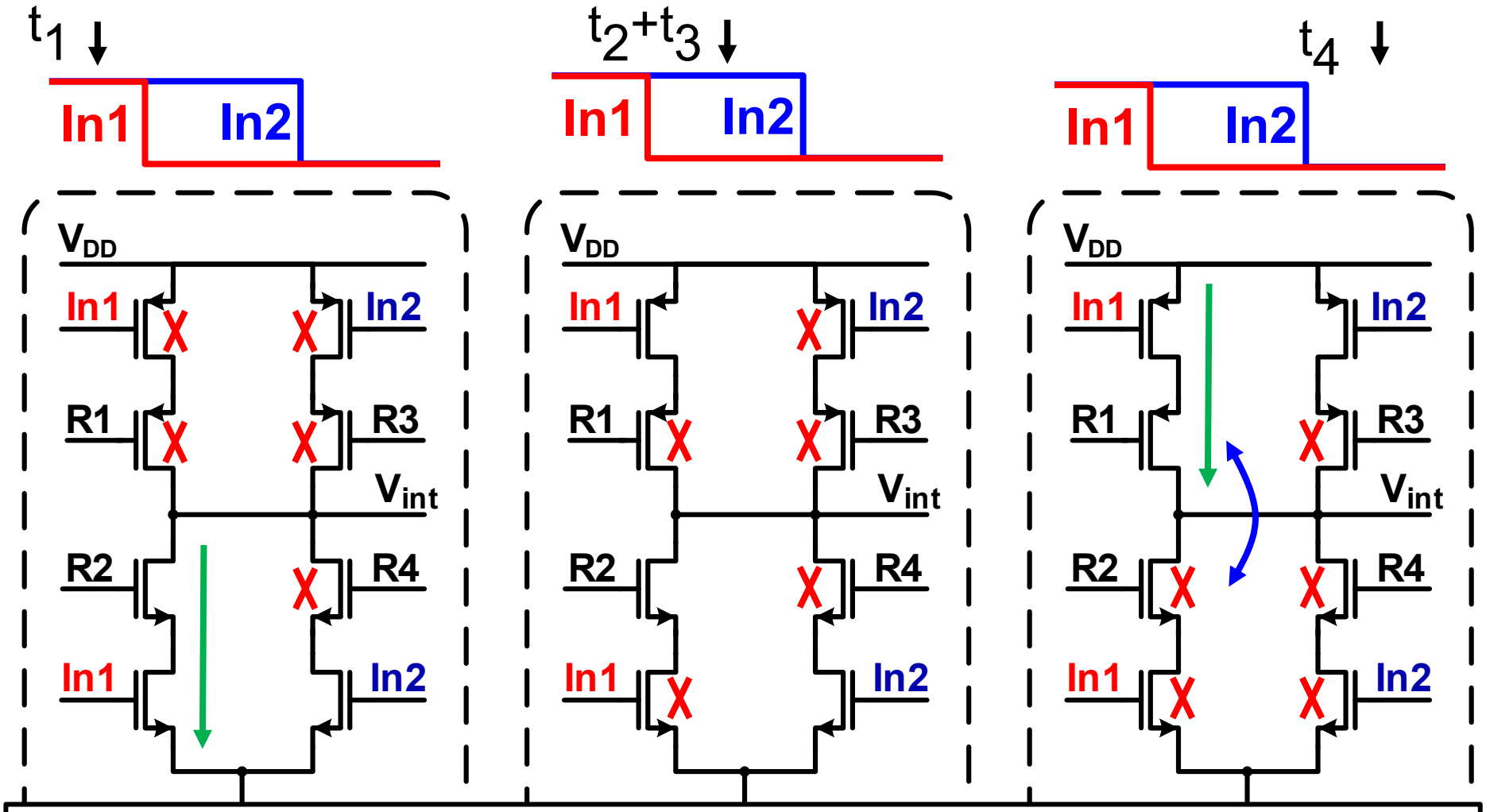
2.6 Retention Cells (2/3)



t_2+t_3: Interpolation in progress

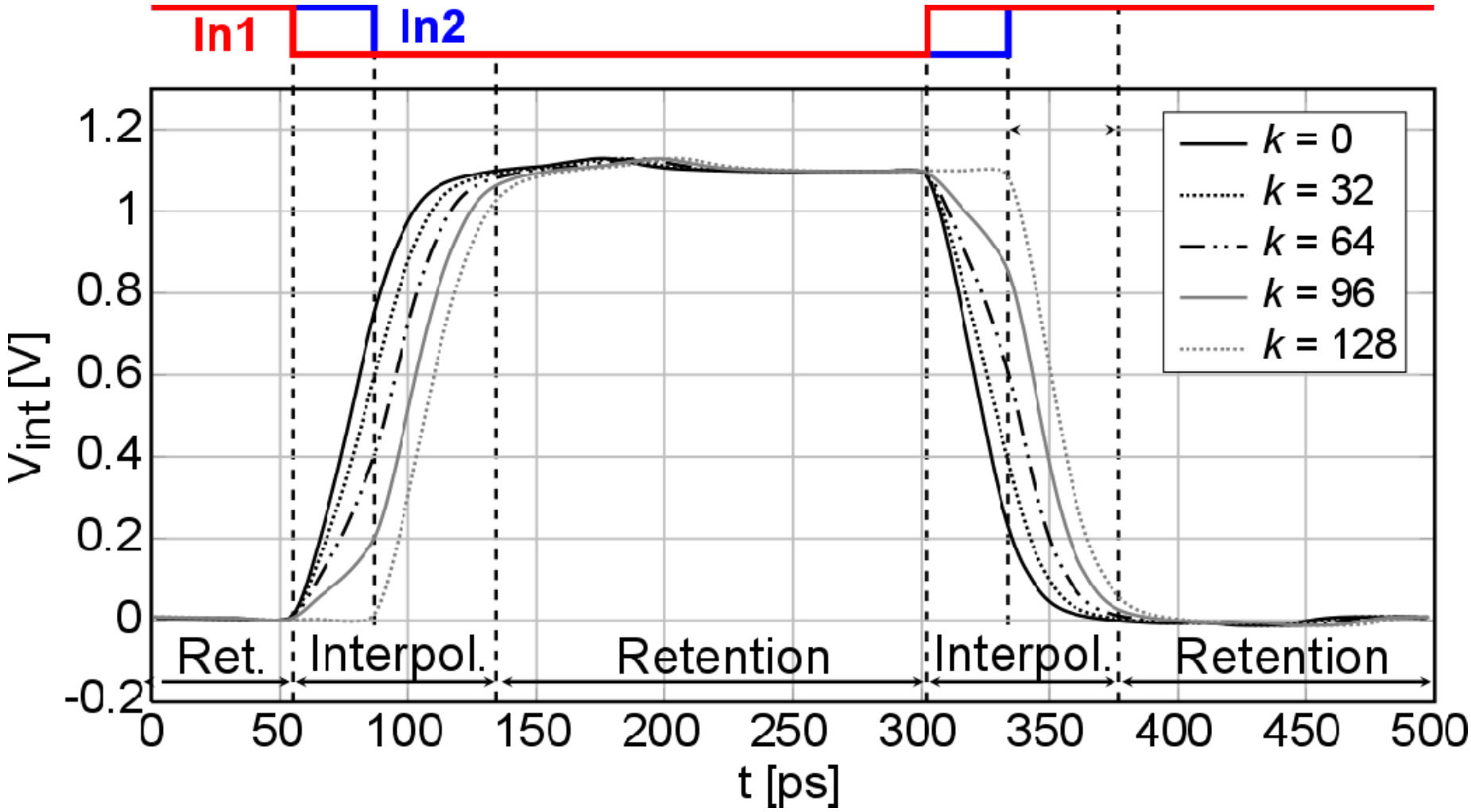
- Retention cells disconnected from V_{int} during interpolation

2.6 Retention Cells (3/3)

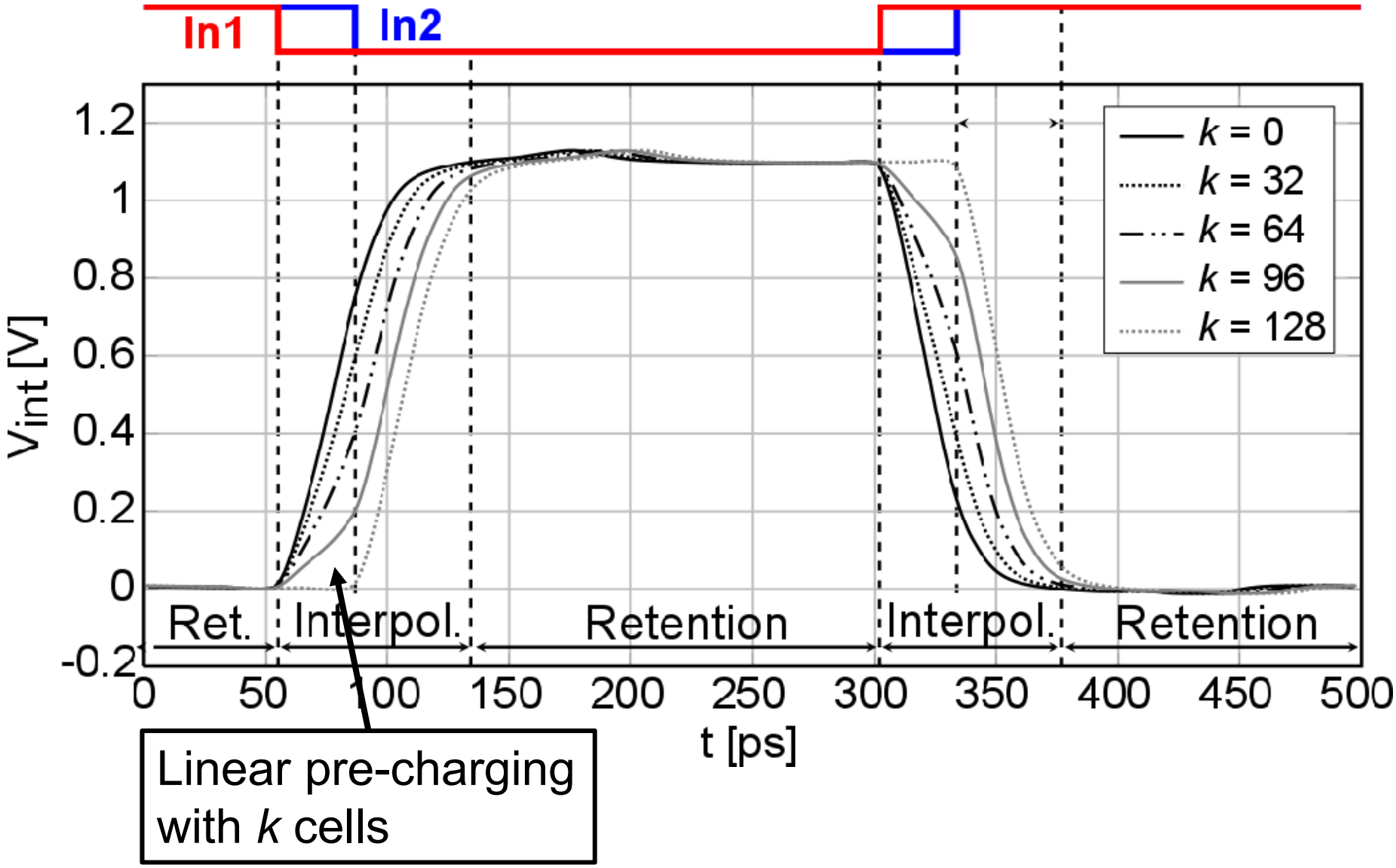


Cell internal logic switches R1,3 to R2,4 with feedback from V_{int}

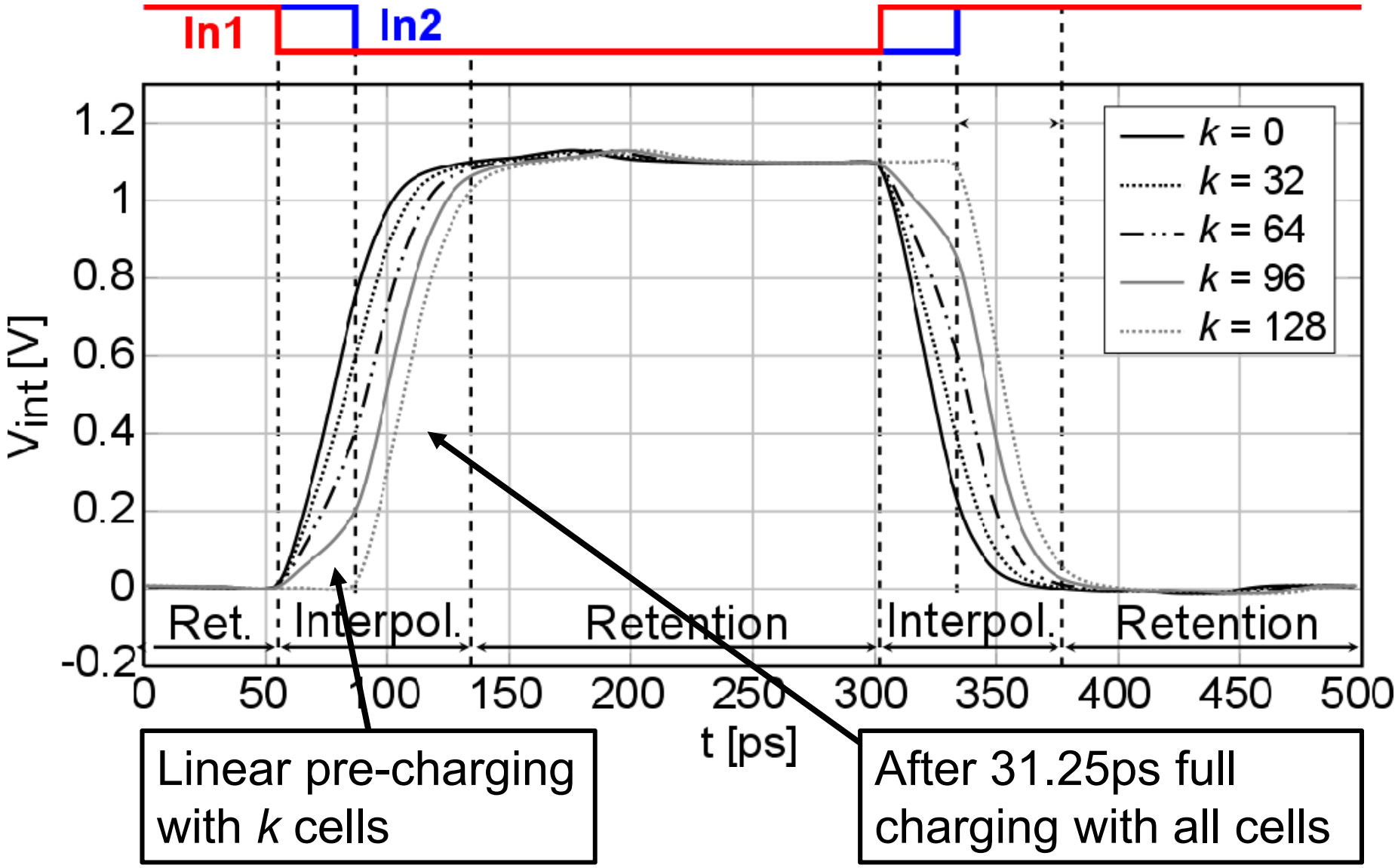
2.7 Simulated Interpolation



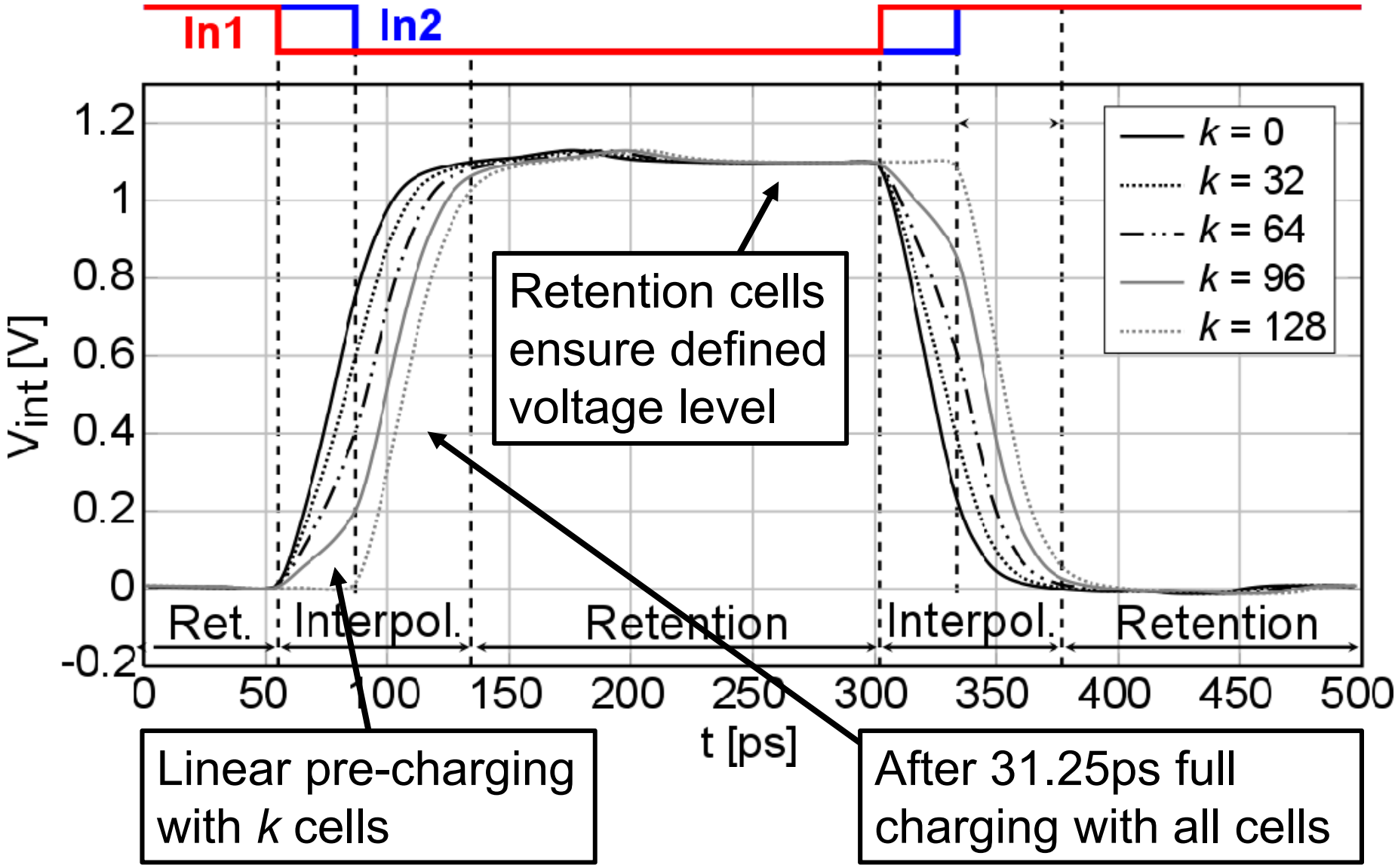
2.7 Simulated Interpolation



2.7 Simulated Interpolation



2.7 Simulated Interpolation



3. Measurement Results

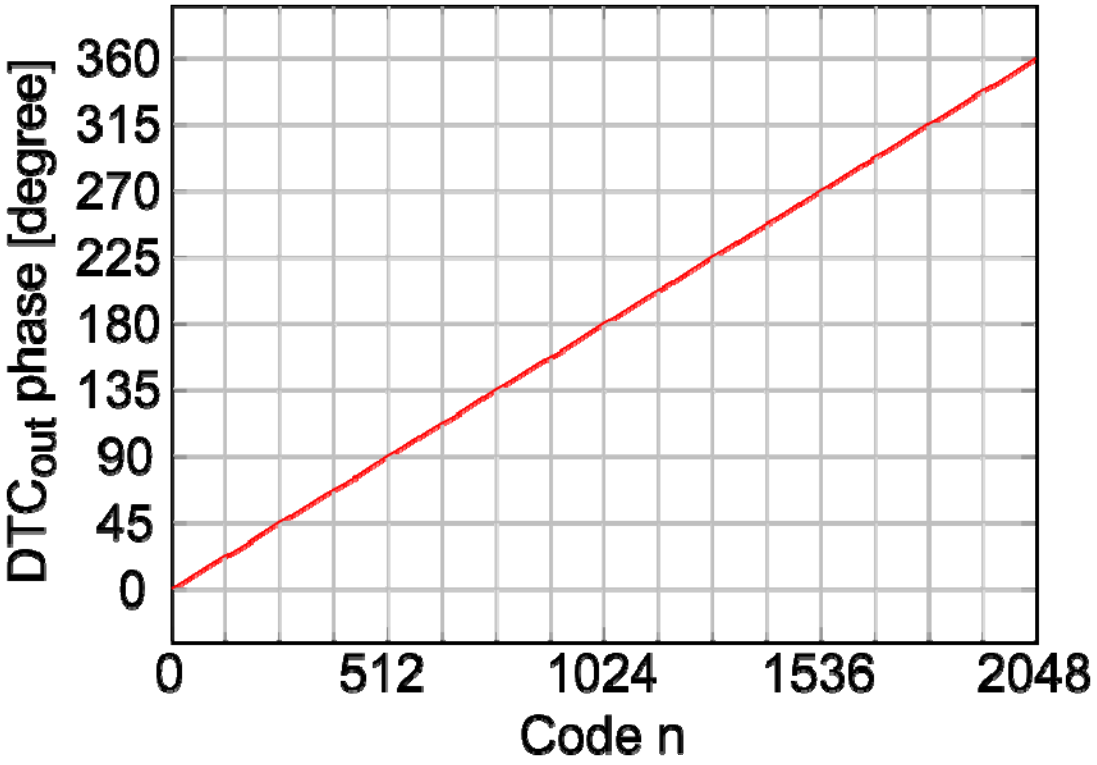
- DTCs are D/A converters, where the analog domain is time or phase
- Most interesting are therefore:
  - Behavior of digital input code vs. output phase
  - Dynamic range
  - Differential nonlinearity (DNL)
  - Integral nonlinearity (INL)
- Phase noise (PN) or jitter are also of interest
- For all measurements: $360° \mathrel{\widehat{=}} 500ps = T_{2GHz}$

3.1 Transfer Function (TF)

TF definition:
TF[n] is the measured DTC output phase at code n, normalized to the phase at $n = 0$.
$n \in \{0,1, \ldots, 2^{11} - 1\}$

The DTC's output phase can only be measured relative to a reference, not absolute!

Dynamic Range: 2π

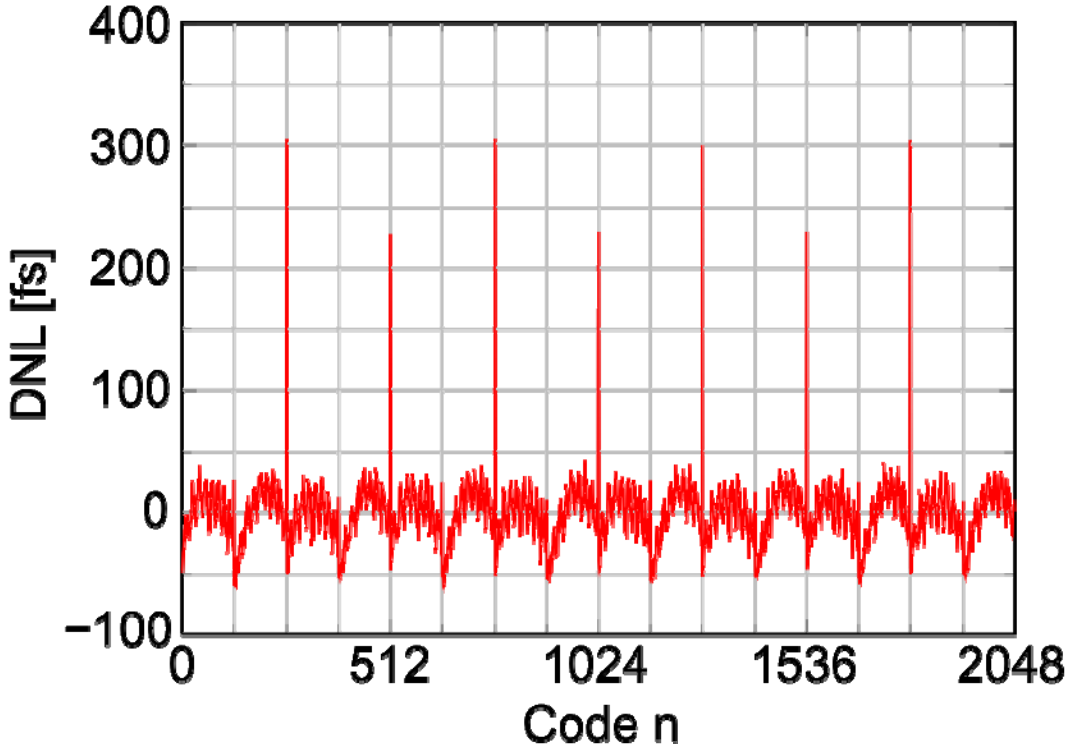


3.2 Differential Nonlinearity (DNL)

DNL definition:

$$\mathrm{DNL}[n] = \mathrm{TF}[n+1] - \mathrm{TF}[n] - 1\mathrm{LSB}$$

$$n \in \{0,1,\ldots,2^{11}-2\}$$



Peak DNL: 305fs
1.25LSB
Fully monotonic

- DNL measures nonlinearity of the step sizes
- Nonlinearity repetitive
  - Repeats by construction all 512 codes
  - Re-alignment of MMD with different VCO cycles

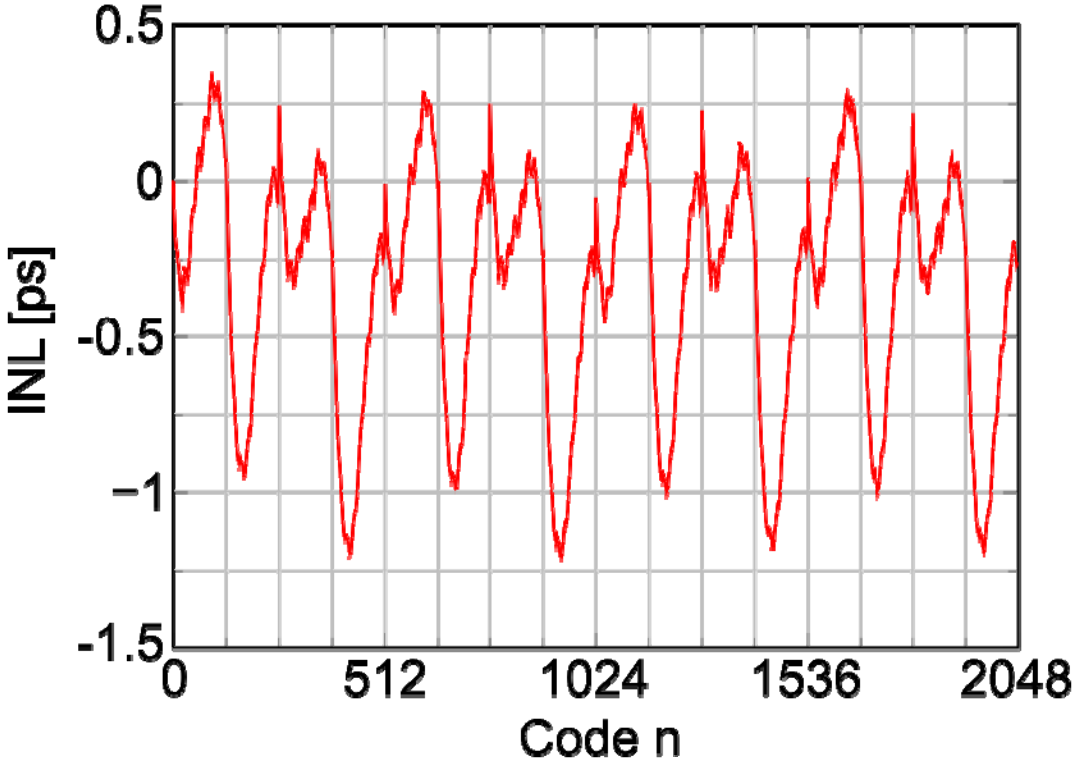
3.3 Integral Nonlinearity (INL)

INL definition:

$$\mathrm{INL}[n] = \mathrm{TF}[n] - n \cdot 1\mathrm{LSB}$$

$$n \in \{0,1,\ldots,2^{11}-1\}$$

Peak INL:	1.2ps
	4.9LSB

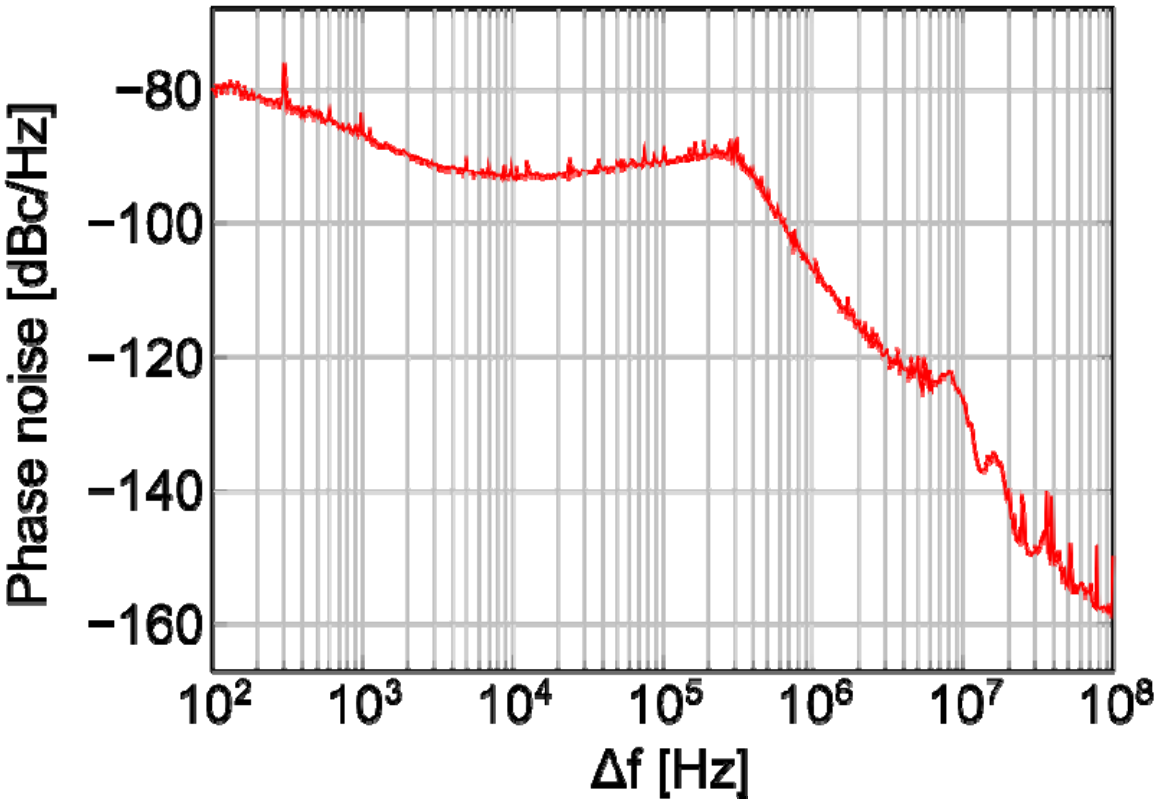


- INL measures absolute nonlinearity at each code
- Nonlinearity repetitive as in DNL

3.4 Power and Phase Noise (PN)

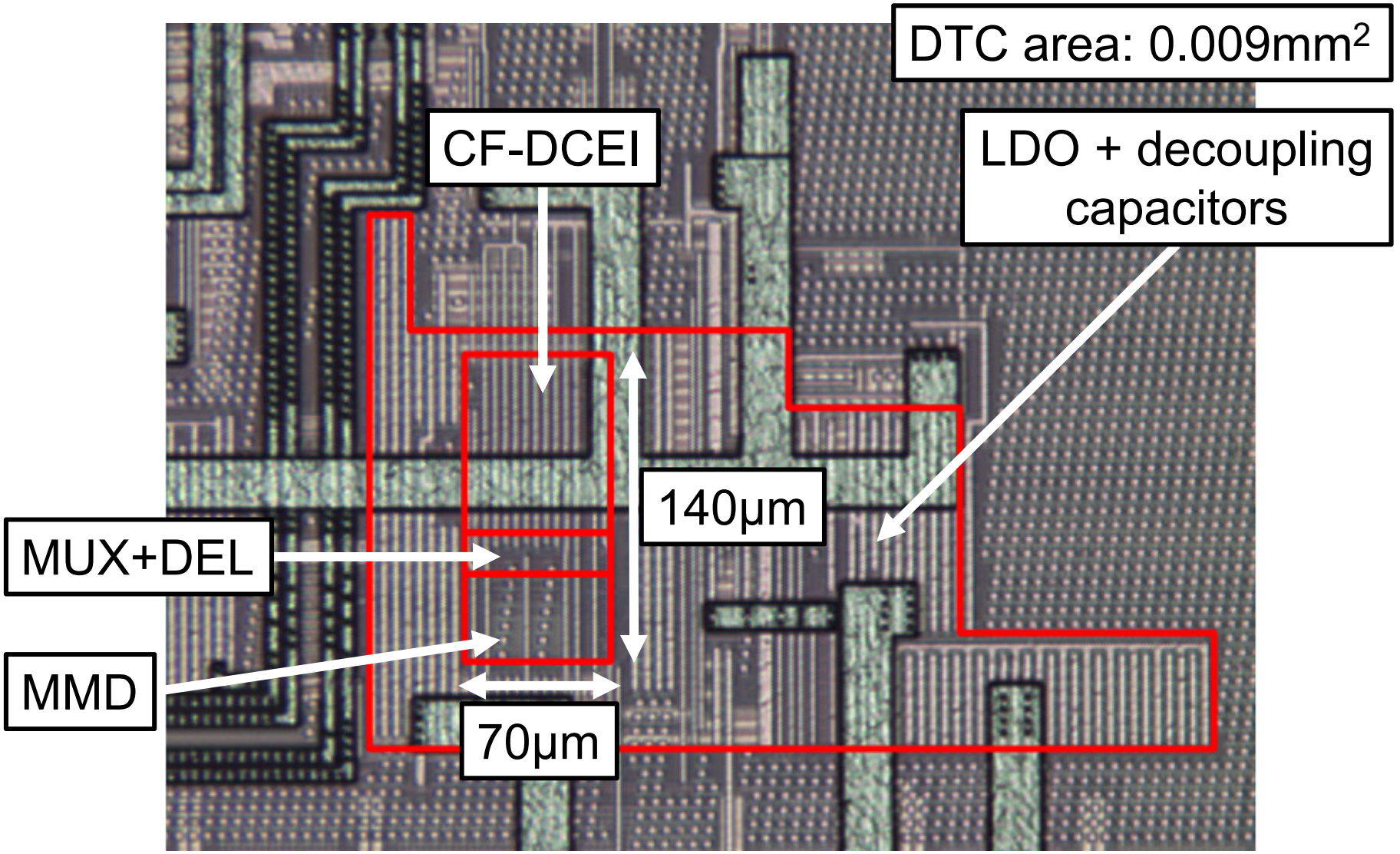
Current from 1.1V:
- MMD: 5mA
- MUX+DEL: 2mA
- CF-DCEI: 11mA

PN at 100MHz offset from 2GHz carrier: -159 dBc/Hz



- PN is mostly dominated by noise from the PLL
- Far-out noise floor is of interest

3.5 Die Micrograph



4. Summary

- 11b DTC, operating at 2GHz
  - Divider based coarse tuning with 2π dynamic range
  - Linearized interpolation based fine tuning on rising and falling edges
- Peak DNL = 305fs, peak INL = 1.2ps
- Far-out PN floor: -159 dBc/Hz (at 100MHz offset)
- Implemented in 28nm CMOS at 1.1V supply
  - Area of 0.009mm²

Stage	MMD	MUX+DEL	CF-DCEI
Resolution	3b (62.5ps)	1b (31.25ps)	7b (244fs)
Current	5mA	2mA	11mA

List of References

- [1] M.-S. Chen et al., “A 0.1–1.5 GHz 8-bit Inverter-Based Digital-to-Phase Converter Using Harmonic Rejection,” IEEE J. Solid-State Circuits, vol. 48, no. 11, pp. 2681-2692, Nov. 2013.
- [2] P. Hanumolu et al., “A Sub-Picosecond Resolution 0.5–1.5 GHz Digital-to-Phase Converter,” IEEE J. Solid-State Circuits, vol. 43, no. 2, pp. 414-424, Feb. 2008.
- [3] J. Ru et al., “A High-Linearity Digital-to-Time Converter Technique: Constant Slope Charging,” IEEE J. Solid-State Circuits, vol. 50, no .6, pp. 1412-1423, June 2015.

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- [4] N. Markulic et al., “A 10-bit, 550-fs step Digital-to-Time Converter in 28nm CMOS”, European Solid State Circuits Conf., pp. 79-82, Sept. 2014.
- [5] A. Ravi et al., “A 2.4-GHz 20–40-MHz Channel WLAN Digital Outphasing Transmitter Utilizing a Delay-Based Wideband Phase Modulator in 32-nm CMOS,” IEEE J. Solid-State Circuits, vol. 47, no. 12, pp. 3184-3196, Dec. 2012